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Compensated Single Input Multiple Output Flyback Converter

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Abstract: A new single-input multiple-output (SIMO) converter is proposed in this work by incorporating flyback and buck converters in a master–slave configuration. The objective of this work is to address the cross regulation problem, achieve tight voltage regulation, improve the circuit form factor and attain a fast transient response for a SIMO flyback converter. The flyback converter maintains the output channels within 10% of their rated voltages and the SIMO buck converter is placed in series with the flyback converter such that it compensates for the output voltage deviation. Moreover, a time multiplexing switching scheme decouples output channel to eliminate the cross-regulation problem and remove the need for an additional winding transformer per each output channel. A type II compensator with a peak current mode controller was designed to achieve faster transient response which is critical for the proposed configuration. A thorough steady-state analysis was carried out on a triple output channel topology to obtain the design criteria and component values. MATLAB/Simscape modelling and simulation was used to validate the effectiveness of the proposed converter with the result yielding satisfactory transience even with load disturbance. Additionally, the result of the proposed converter is compared with previously published works.

Keywords: dc-dc converter; SIMO power supply; series compensation; cross regulation

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1. Introduction

The advancement in Electrical Vehicles (EVs), grid technology, medical instrumentation, military technology, building and factory automation has led to a high demand of dc–dc converters with galvanic isolation and multi-channeled output. For instance, an isolated converter is necessary in EVs to prevent faults in power stages from damaging the control electronics that control them. On the other hand, there are several types of loads such as electrical engines, entertainment dashboards, air conditioning and lights that require different power conditions. The primary goal of a multiple output DC/DC converter is to offer an efficient, compact and simple power supply that accommodates different load conditions at the same time. The simplest but not the most efficient topology is conventionally formed by incorporating N independent converters to drive N outputs. Although this configuration offers simplicity, effective performance and independent control, the final product is bulky and costly especially when galvanic isolation is necessary. Indeed, the overall form factor and converter cost is impaired when one switching mode power supply (SMPS) transformer is needed per each isolated converter. A flyback converter is an isolated converter topology that is being used widely in low power applications because of its simple structure, low component counts and possible step down/step up voltage operation. Multiple output configuration is simply achievable in flyback converter by incorporating multiple winding SMPS transformers. Figure 1 shows a SIMO flyback converter in which any output can be made the "master" by connecting it directly to the feedback control loop (e.g., output 2), and the other one (s) as "slave" by fine-tuning the turn ratio of the tertiary winding [1,2]. Although this setup is easy to implement, cross-regulation issue arises from differences in leakage inductances of secondary and tertiary

winding, and consequently, this reduces the accuracy of the output voltages. To overcome this, a popular approach in industrial applications is to sense all outputs and base the regulatory control on a combination of the feedback loops. Though this method improves regulation, the approach in which the main output has its own feedback will be better regulated relative to the outputs based on combinatory feedback control. Therefore, the overall output error remains unchanged and it only shifts among channels. To further address the cross regulation problem, a secondary side and low drop-out post regulators are adopted [3–5]. Although linear regulatory schemes yield tight regulation, they are inefficient due to the voltage drop across the regulator and as such not appropriate for low output current application. The magamp technique is presented in [6,7], for the flyback converter and much effort has been devoted to improve the PWM feedback performance of the main output which had been restricted to the output with higher voltage. However, a minimum load is essential to attain desired regulation as leakage and saturated inductances still impact critical operating conditions.

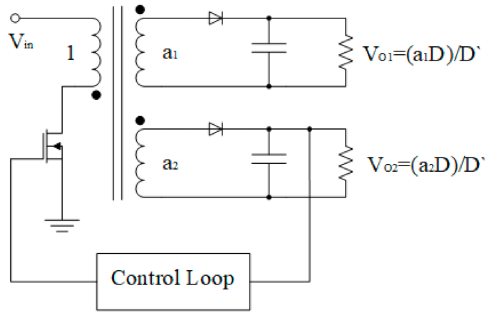

Figure 1. A typical regulated flyback converter.

Endeavors have been made in [8–12], to eliminate the cross-regulation problem by incorporating multiple linear regulators, where efficiency and control simplicity are sacrificed at high load current and frequency. In [13], a non-isolated SIMO converter is designed based on a coupled conductor which works on one high-voltage output channel and multiple middle-voltage output channel. While the high-voltage output channel is controllable by a simple PI controller, the middle-voltage output channel should be adjusted by the design of an additional auxiliary inductor for the desired voltage level and load current. In the work by Prieto et al., 16 different non-isolated SIMO topologies were compared, and their main features discussed [14]. In addition, a three output non-isolated converter is developed based on a single-ended primary inductance (SEPIC)–Cuk–Boost combination. The new combination topology is derived from identical front end of other converters, which is single switch with only one inductor. The proposed method is interesting for the applications that have different load requirements, and they should be integrated as a system. However, it could not be adopted as an isolated converter topology due to the cross-regulation problem among the combined converters.

The objective of this paper is to develop a SIMO power supply based on a flyback converter, to achieve independent output control, no cross regulation and minimal deviation on output voltages. A new hybrid configuration will be proposed in this paper, which utilizes a flyback converter as the main converter to reach the rated voltage and an additional small SIMO buck converter to reduce output voltage deviations. In this work, a time-multiplex switching scheme as reported in [15,16], is employed to regulate multiple outputs by using only a three-winding SMPS transformer. This will serve to reduce the overall converter footprint, as well as to eliminate the cross-regulation issue.

This research further analyzes the conventional technique for multiple output flyback converters in Section 2 and the new topology is developed thereafter. The operating principle along with a timing diagram for the switches is illustrated in Section 3. For simplicity and clarity, a two-output power supply is used to break-down the proposed control methodology and subsequently extended to a three-output power supply by adopting high

frequency time sharing technique for series compensation. Selection of key components for flyback and buck converters and design considerations are detailed in Section 4. Flyback converter control circuit design is discussed further for peak current mode control and the circuit stability is examined by proving the transfer function and plotting the bode plot. Simulation results are presented for a triple output power supply in Section 5, which validate the effectiveness of employing series compensation to achieve 1% voltage regulation. Transient response of the converter to 20% load variation is studied and robustness of the control circuit is shown. Lastly, Section 6 provides a synopsis of the main results and the contributions of the paper.

2. Configuration Derivation

In this work, independent control over the output channels of the flyback converter is achieved by the time-multiplexing switching scheme reported in the abovementioned work. The switching scheme is such that each channel has an isolation switch which isolates the outputs during its charging periods. The isolation switches (Q_1 and Q_2) operate at a lower frequency relative to the main switch of the flyback converter so as to provide enough regulation time per channel. Necessarily the duty cycle of isolation switches is not equal and it is dictated by the channel's load condition. Q_n regulates one channel at a time during an on-time cycle of the associated isolation switch. As a result, channels are regulated independently, and each can operate under different load conditions (voltage and current). In this configuration, the size output capacitance is not solely a function of load requirement but also the number of output channels. In fact, with an increase in the number of output channels, more output capacitances are needed to attain the desired output voltage deviation. A SIMO converter based on flyback topology is proposed in [17], to overcome this drawback, which also eliminates cross regulation issue. The key idea lies under the provided galvanic isolation, which allows the injection of series voltage with the output capacitors for voltage compensation and improving the regulation index. Indeed low-power buck converters that are placed in series with filter capacitors properly compensate for voltage decrease during the off-time cycle of isolation switches. In this work, advancements were achieved as a continuation of previous aforementioned work by consolidating all buck converters and using single shared inductors and eliminating additional power sources for the series compensation by adding the low-power tertiary transformer winding. Figure 2 depicts the proposed multiple-output power supply circuit. Relative to a conventional multiple output power supply circuit, a two windings configuration is sufficient for primary regulation and the tertiary winding is required for series voltage compensation.

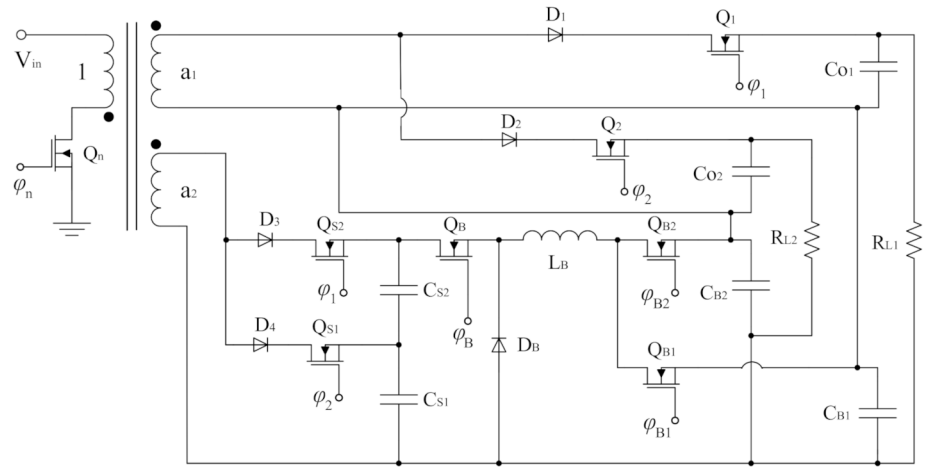

Figure 2. Topology of the proposed single-input multiple-output (SIMO) power supply based on the master-slave topology.

Indeed, the quaternary windings which is required for a typical triple output flyback converter has been removed, an isolation switch is added instead per additional channel and in turn the overall form factor is improved. The principle of operation of the low power multiple output buck converter in series with the flyback converter will be covered in Section 3.

Figure 3 shows the topology of the SIMO power supply without buck converter series compensation. For simplicity, the timing scheme of this configuration is discussed first and then the discussion will be extended to the proposed topology. The switching frequency (*Fs*) of the Q_n is set to be higher than the switching frequency *(Fo)* of the isolation switches (Q_1 and Q_2). An appropriate F_O is selected based on a compromise between switching loss, load current and output capacitor size. The total regulation time period T_O ($1/F_O$) should be split among N output channels and here for the sake of simplicity it is divided into N equal intervals and each is assigned to a channel as its regulation time period.

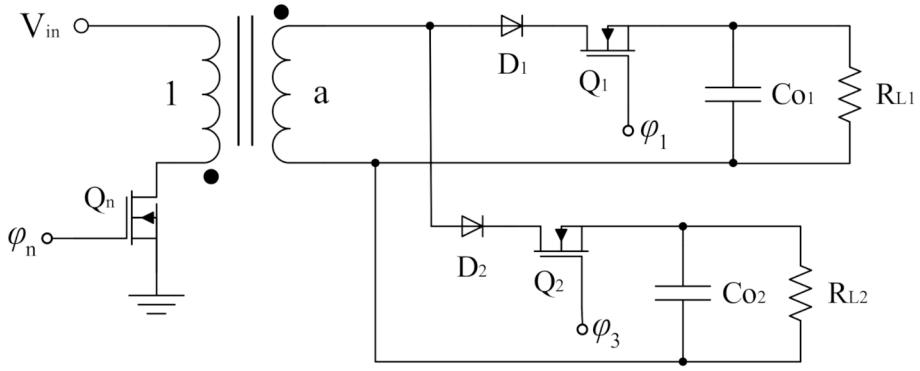

Figure 3. Topology of the proposed SIMO power supply without series compensation.

The isolation switching signal associated with q_n is regulated to have a duration of $T_n = \beta_n$ *(To/N)* and a time shifting of T_{shf} = To $(n-1)/N$, where β_n is a factor to implement dead time logic among master converter's outputs and is less than one:

$$\mathrm{T_n} = \beta_\mathrm{n}.\left(\frac{\mathrm{T_O}}{\mathrm{N}}\right) = \frac{\mathrm{T_O}}{\mathrm{N}} - \mathrm{t_{n5}} \tag{1}$$

In order to remove the interference among the flyback converter's channel, the secondary charging current of the flyback transformer should reach zero before the next channel starts to regulate. The time required for the charging current in the transformer secondary to reach zero is denoted as the charging current reset time (t_{n4}).

$$\mathrm{T_{nO}} = \mathrm{T_n} - \mathrm{t_{n4}} \tag{2}$$

By this timing scheme, the last charging signal of the flyback converter that belongs to channel number *n* could be sent before the end of T_{n0} and the secondary charging current of the flyback transformer is guaranteed to reach zero by the end of T_n. Hence, each channel is regulated within about *1/N* of the total regulation time period (*To*) and, subsequently, the channel will be disconnected from the flyback converter and its output capacitor (C_{on}) takes over the load. The output capacitor should, therefore, be sized to be able to service the load for the remainder of the interval which is about *To* $(N-1)/N$. The needed capacitance can be calculated by using the equation below:

$$C_{on} = \left(\frac{N-1}{N}\right).\frac{I_{on}}{F_o.\Delta V_{on}} \tag{3}$$

where I_{on} and ΔV_{on} are the load current and output voltage deviation of the channel number *n*, respectively. According to Equation (3), for a given load current and number of channels,

Fo should be increased to lower the size of output capacitors and attain tight regulation. The highest achievable isolation switching frequency is a function of the main switching frequency (*Fs*) of the flyback converter. However, higher *Fs* results in higher transformer loss and the usual compromise is switching within 100–500 kHz. Furthermore, the highest achievable isolation switching frequency could be reduced to 15–45 kHz by factors such as the number of output channels, slew rate of converter, the charging current reset time, and more importantly, the duration required by the flyback converter in order to regulate a single output channel during an on-time interval (*Tn*), which is at least 5–10 times the switching period of the main converter. Consequently, this topology is best suited for applications with a low number of output channels, low load current and high voltage.

The proposed converter shown in Figure 2 can address the aforementioned challenges thanks to the galvanic isolation of the flyback converter and the in-series buck converters with the output capacitors (C_{on}). The proposed control strategy in [18], is employed for a series compensation circuit to configure a single inductor multiple output buck converter. The tertiary winding of the flyback transformer supplies the input voltage of the buck converter. Its turn ratio in conjunction with the adopted control strategy should be designed such that the maximum possible voltage compensation of the buck converter is limited to a relatively small value (e.g., 1 V). Step-down topology for the compensator converter (buck topology) along with its 1 V input power supply limit the voltage range of C_{Bn} between 0 and 1 V. Given the range of possible voltage compensation by the buck converter and the voltage decay across C_{On} during its flyback converter turn OFF time interval, it can be concluded that the buck converter would never cause over-regulation. This technique restrains power usage of the buck converter, and as a result it provides a small overall form factor. It can be shown that the rated output power of buck regulator is about 1/50 that of the flyback converter, making on-chip implementation possible for the buck regulators. When each channel's flyback converter is regulating its output, the corresponding switching signal of the buck converter is turned off. As soon as the flyback converter switches to regulating the next output channel, the series buck compensation circuit of the previous channel becomes activated and starts regulating its output. This regulation strategy ensures the tight regulation of each output. Relative to previous configurations, the complimentary buck regulator allows smaller output capacitors to be used for the flyback converter. The proposed topology employs closed loop feedback control for compensation, provides independent output control with tight regulation and eliminates cross-regulation.

3. The Principle of Operations

This section covers the detailed steady state analysis of the proposed SIMO power supply with two output channels. For an N-channeled system, the results obtained in this section can be easily developed. For simplicity, parasitic parameters such as including on-resistances of switches, the transformer's DC resistance and equivalent series resistance (ESR) of capacitors are neglected. The timing scheme shown in Figure 4 can be applied to any converter mode of operation like a continuous conduction mode (*CCM)* or discontinuous conduction mode (*DCM*).

Since the *DCM* operation of the flyback converter causes greater charging current value than the *CCM* operation, in the following calculations *DCM* was adopted to calculate the charging current reset time as the worst case. To cover the operations of the flyback and buck converters separately, two different time scales were established. Subsequently, by using several equivalent circuits, the principle of operations for the first output channel within a 0–*To*/2 time interval will be described in detail.

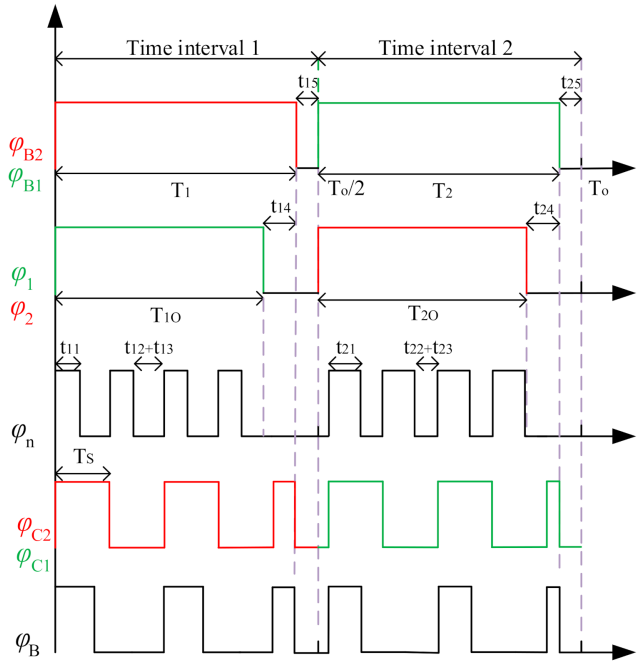

Figure 4. Timing diagram of the proposed single-input multiple-output power supply.

3.1. Time Interval 1 (0~To/N)

Channel 1 is regulated by the flyback converter in this time interval while the correspondent buck converter is shut off to allow C_{B1} contributes to driving the load and more importantly be discharged as much as possible. This technique provides the maximum and fastest series compensation for the next cycle because buck converter's feedback loop generates the maximum error signal and the controller considers that as an extremely hard load transient. During this time interval, channel 2 is disconnected from the flyback converter and the series compensator reacts quickly to the error signal and charges C_{B2} to compensate C_{O2} voltage drop.

To further analyze main regulation of channel 1 and series regulation of channel 2, this interval is broken into five subintervals.

3.1.1. Flyback Converter Analysis

(a) Time Span $t_{11} = d_{11}\ T_s$

During this time span, Q_n is close and the energy from power supply is stored in the transformer (Lm). Q_1, Q_{S2} and Q_{B2} are close, and diode D_1 and D_3 are reverse biased. Figure 5 depicts the equivalent circuit of the proposed SIMO converter over this time span. Main and series regulations are discussed separately as follows per each time span.

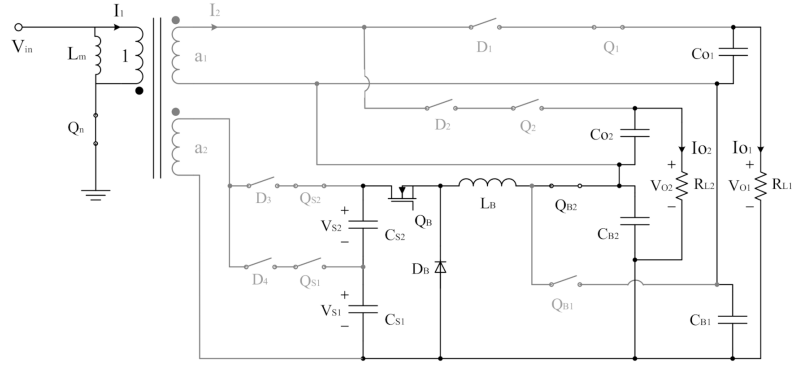

Figure 5. Equivalent circuits of the proposed SIMO power supply within T1–t11.

Main Regulation:

In steady state, the expression of input current, magnetizing current and dc gain are presented as below [19]:

$$I_1 = \frac{-I_2}{a_1} = 0 \tag{4}$$

$$\Delta I_{Lm} = I_{Lm_{(max)}} = \frac{V_{in}}{L_m} d_{11} T_s \tag{5}$$

$$M_{VDC} = \frac{V_{o1}}{V_{in}} = \frac{d_{11}}{a_1 d_{12}} \tag{6}$$

where a_1, d_{11} and $d_{12}T_s$ are the transformer turn ratio, duty cycle of the flyback converter for channel 1 and time needed for I_2 to reach zero, respectively.

Series Regulation:

During this time interval the channel 2′s series buck converter is fed by the series connection of C_{S1} and C_{S2}. Q_{S2} could be switched by φ_1 or φ_2. The selection between φ_1 and φ_2 depends on the output voltage level. Indeed, Q_{S2} should be controlled with the switching signal associated with the higher voltage output channel. This is because Q_{S2} adjusts the series voltage over C_{S1} and C_{S2}, while Q_{S1} just controls the voltage over C_{S1} and the induced voltage is a function of a_2 and duty cycle of Q_n. It has been shown in [20], that practical global stability can be achieved in DC/DC converters with simple integral control. Hence, in the proposed Buck Converter Control Circuit (BCCC), the integration of the output voltage is used as control signal in Figure 6. Detail buck converter analysis is presented in the next section. The switching frequency of the buck converters is equal to that of the flyback converter to minimize electromagnetic interference (EMI). Q_{B2} is triggered with φ_{B2}, and as a result it stays close as long as the other channels are conducting. The buck converter regulates C_{B2} to compensate C_{O2}′s voltage drop. In order to achieve tight regulation of channel 2, C_{B2} needs to be discharged while its flyback converter is in turn-ON time interval ($T_O/2$~T_O), so that C_{B2} in return achieves maximum voltage increase while the buck converter is in turn-ON time interval (0~$T_O/2$). Hence, as long as C_{B2} is charged during T_1, the voltage reduction of C_{O2} would be compensated, and the load voltage (V_{O2}) would stay tightly regulated. In order to achieve high frequency time sharing technique in [18], switching signal φ_{C1} in Figures 4 and 6 is generated such that just one buck converter is regulated during T_s. For instance, regulation frequency of the buck converter in a two-channel topology within T_n is (1/2) F_s, and in a three output channel topology is (1/3) F_s.

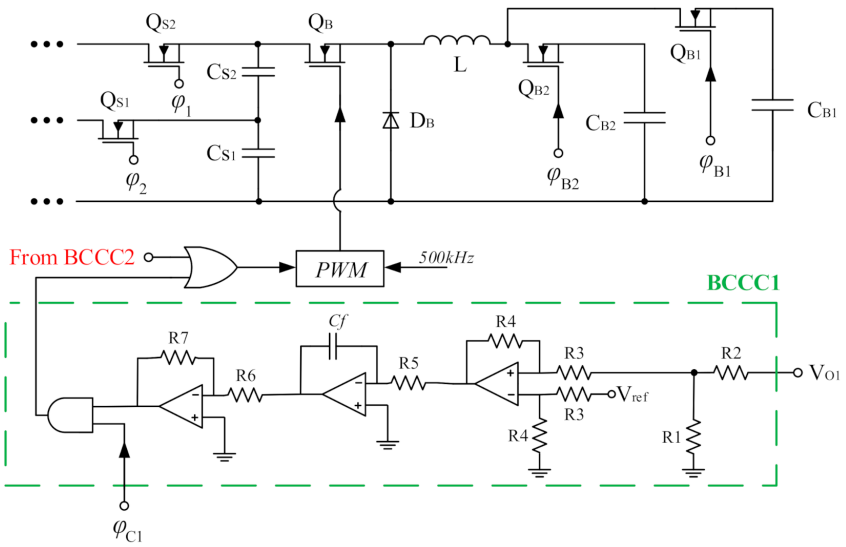

Figure 6. Closed loop model of the buck converter.

(b) Time Span $t_{12} = d_{12}\ T_s$:

In this time span Q_1 and Q_{S2} stay closed within t_{12} and by sending a turn-OFF pulse to Q_n, diode D_1 and D_3 start to conduct and allow the stored energy in L_m to be transferred to the load. Figure 7 depicts the equivalent circuit of the proposed SIMO power supply over this time span.

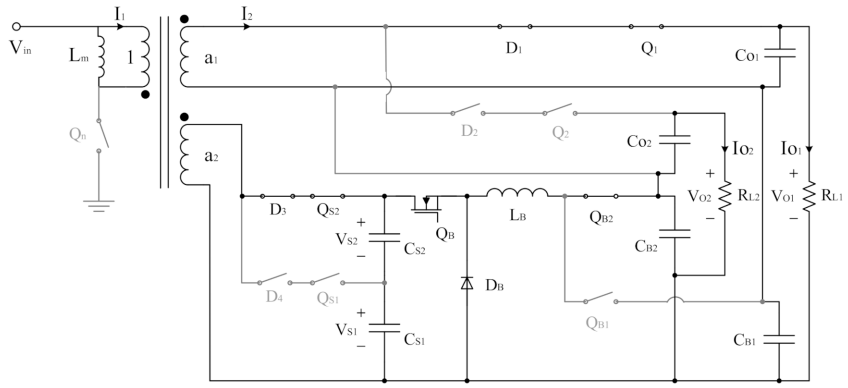

Figure 7. Equivalent circuits of the proposed SIMO power supply within T1–t12 and t14.

Main Regulation:

The equations for the secondary current are shown below [19]:

$$I_2 = -a_1 I_1 = a_1 I_{Lm} = \frac{-a_1{}^2 V_{o1}}{L_m}(t - d_{11}T_s) + \frac{a_1 V_{in} d_{11}}{F_s L_m} \tag{7}$$

Thus:

$$I_{2(max)} = \frac{a_1 V_{in} d_{11}}{F_s L_m} \tag{8}$$

Using Equation (4), the dc current is given as:

$$I_{o1} = \frac{1}{T_S}\int_0^{T_S} I_2 dt = \frac{1}{T}\int_{d_{11}T_s}^{(d_{11}+d_{12})T_s} I_2 dt = \frac{d_{11}a_1\Delta i_{Lm}}{2} = \frac{a_1 d_{11} d_{12} V_{in}}{2F_s L_m} = \frac{V_{o1}}{R_{L1}} \tag{9}$$

It yields:

$$\frac{V_{o1}}{V_{in}} = \frac{a_1 d_{11} d_{12} R_{L1}}{2F_s L_m} \tag{10}$$

Combining Equations (7) and (9), results in:

$$d_{11} = \left(\frac{V_{o1}}{V_{in}}\right)\sqrt{\frac{2F_s L_m}{R_{L1}}} \tag{11}$$

$$d_{12} = \sqrt{\frac{2F_s L_m}{a_1{}^2 R_{L1}}} \tag{12}$$

Substituting Equation (11) in Equation (6),

$$I_{2(max)} = a_1 V_{o1}\sqrt{\frac{2}{F_s L_m R_{L1}}} \tag{13}$$

Series Regulation:

D_3 starts switching simultaneously with the D_1 as a slave flyback converter. Therefore, in the steady state the slave flyback converter regulates the voltage across C_{S1} and C_{S2} in terms of $C_{O1'}$s voltage as below:

$$V_{S2} + V_{S1} \approx \frac{a_2}{a_1}.V_{O1} \tag{14}$$

Q_{B2} remains closed and the buck converter continues to compensate $C_{O2'}$s voltage drop by regulating C_{B2}. Note that during time interval 2 (To/2~To), Q_{S2} is close and Q_{S1} is open. As a result, this time D_4 starts switching simultaneously with the D_2 as a slave flyback converter and the voltage across C_{S1} could be obtained as follow:

$$V_{S1} \approx \frac{a_2}{a_1}.V_{O2} \tag{15}$$

The voltage across C_{S1} can be derived from Equations (13) and (14) as below:

$$V_{S2} = \frac{a_2}{a_1}.(V_{O1} - V_{O2}) \tag{16}$$

Assuming:

$$V_{O2} = x.V_{O1}\ and\ x < 1 \tag{17}$$

Consequently:

$$\frac{C_{S2}}{C_{S1}} = \frac{V_{S1}}{V_{S2}} = \frac{x}{1-x} \tag{18}$$

On the other hand, the parallel connection of C_{S1} and C_{S2} should be large enough for the designed line regulation of the buck converters.

(c) Time Span $t_{13} = (1-d_{11}-d_{12})\ T_s$

Main Regulation:

When Q_n and D_1 are open, the secondary charging current I_2 is zero and C_{o1} is effectively in series with C_{B1} and the equivalent capacitance supplies the load. One switching cycle of the flyback converter is completed at the end of this time span which takes $(1-d_{11}-d_{12})\ T_s$ long. The elapse of time interval T_{1O} occurs after the completion of multiple time spans t_{11}, t_{12} and t_{13} occurred for $N_{itr} = T_1/T_s$ iterations. The equivalent circuit of the master–slave converter configuration at t_{13} time span is depicted in Figure 8.

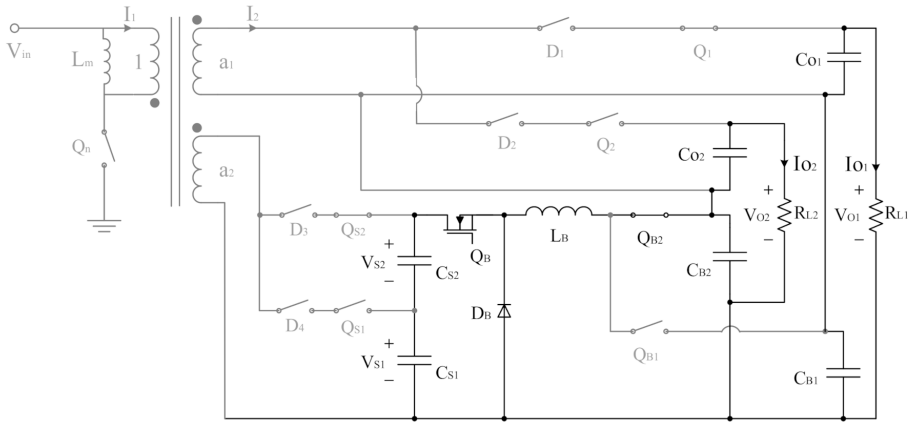

Figure 8. Equivalent circuits of the proposed SIMO converter within T1–t13.

Series Regulation:

In this time span, the operation of the buck converter is the same as t_{12}. Due to the delays in the microcontroller control path such as propagation delays, fine-tuning T_{nO} for a specific level of I_2 (e.g., zero current) could be difficult as it may vary with time. Therefore, the necessary time to cover reaching zero secondary current and components delay is split

into two time spans t_{14} and t_{15}. Time span t_{14} is calculated based on the worst-case scenario and t_{15} would be a predetermined setting based on the type of controller.

(d) Time Span t_{14}

Time span t_{14} is the charging current reset time which plays a critical role in eliminating cross regulation problem. The worst case scenario, which assures zero secondary charging current before regulating the next channel, requires the calculation of this time span for the maximum possible secondary charging current ($I_{2(max)}$) at the time of T_{1O}. Time t_{14} is given below based on Equation (11):

$$t_{14} = \sqrt{\frac{2L_m}{{a_1}^2 R_{L1} F_s}} \tag{19}$$

(e) Time Span t_{15}

Delays in microcontroller responses and control loops have been considered in time span t_{15} as a short dead time. During this time span, Q_n is turned off to deactivate the flyback converter while Q_1 and Q_{S2} are also turned off to disconnect the converter from the load. As shown in the Figure 9, all flyback and buck converters are turned off, leaving the series connection of output capacitors (C_{O1}, C_{B1} and C_{O2}, C_{B2}) as the source to supply energy to the loads. Here T_n and T_{n0} are calculated as follows:

$$T_1 = \frac{T_o}{N} - t_{15} = \frac{\beta_1 T_o}{N} \tag{20}$$

$$T_{1o} = T_1 - t_{14} \tag{21}$$

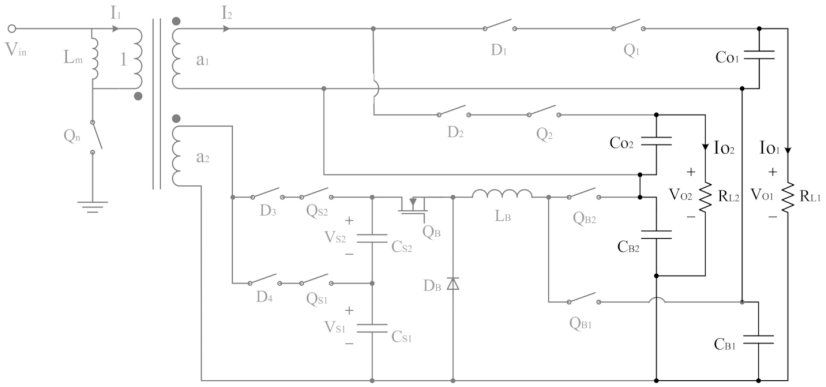

Figure 9. Equivalent circuits of the proposed SIMO power supply within T1–t15.

3.1.2. Buck Converter Analysis

The series buck converter compensates channel 2 throughout T_1. Q_2 is opened in order to disconnect the flyback converter from channel 2, while Q_{B2} is closed allowing normal buck converter operation by proper switching of Q_B and D_B. The maximum possible voltage compensation during T_1 can be calculated when the buck's output capacitor is completely discharged during T_2. The transient response of a buck converter can be rewritten in the S domain. Assuming the series connection of C_{S1} and C_{S2} are large enough to keep V_{Bin} constant within T_1 results in:

$$V_{Bin} = V_{S1} + V_{S2} \tag{22}$$

$$u_2 \frac{V_{Bin}}{S} + L_B i_{L0} - S L_B i_L - v_{B2} - \frac{V_{B20}}{S} = 0 \tag{23}$$

$$v_{B2out} = v_{B2} + \frac{V_{B20}}{S} \tag{24}$$

$$i_L - S C_{B2} v_{B2} - \frac{I_{Load2}}{S} = 0 \tag{25}$$

where u_2—State of Q_{B2} ($u_2 = 0 \geq$ OFF, $u_2 = 1 \geq$ ON) V_{Bin} is the power supply of buck converters, V_{B20} is the initial conditions of the capacitor voltage. Therefore:

$$v_{B2} = \frac{u_2 V_{Bin} - V_{B20}}{S(1 + L_B C_{B2} S^2)} + \frac{L_B(i_{L0} - I_{Load2})}{(1 + L_B C_{B2} S^2)} \tag{26}$$

$$i_L = \frac{u_2 V_{Bin} C_{B2} - V_{B20} C_{B2}}{(1 + L_B C_{B2} S^2)} + \frac{S C_{B2} L_B (i_{L0} - I_{Load2})}{(1 + L_B C_{B2} S^2)} + \frac{I_{Load2}}{S} \tag{27}$$

By taking the inverse Laplace transform, the time-domain expression of V_{B2out} and I_{LB} are as follows:

$$V_{B2out} = \left(\sqrt{\frac{L_B}{C_{B2}}}\right)(i_{L0} - I_{Load2}) \sin\left(\frac{t}{\sqrt{L_B C_{B2}}}\right) + \left(\frac{u_2 V_{Bin} - V_{B20}}{\sqrt{L_B C_{B2}}}\right)\left(1 - \cos\left(\frac{t}{\sqrt{L_B C_{B2}}}\right)\right) + V_{B20} \tag{28}$$

$$I_L = \left(\sqrt{\frac{C_{B2}}{L_B}}\right)(u_2 V_{Bin} - V_{B20}) \sin\left(\frac{t}{\sqrt{L_B C_{B2}}}\right) - (i_{L0} - I_{Load2}) \cos\left(\frac{t}{\sqrt{L_B C_{B2}}}\right) + I_{Load2} \tag{29}$$

Based on the proposed control strategy, duty cycle (D_{B2}) for the buck converter can be expressed relative to the closed-loop gain K and switching time period (T_s) as follows:

$$D_{B2(N+1)} = -K \int_0^{T_s} \left(V_{cc} - V_{refB}\right) dt + D_{B2(N)} \tag{30}$$

where

$$V_{refB} = V_{ref} - V_{Co2}|_{t=0} \tag{31}$$

V_{cc} is the voltage of the control loop integrator. Assuming 1% over-regulation by the flyback converter, the voltage of C_{o2} at the beginning of time interval T_1 is:

$$V_{Co2} = 1.01 \times V_{ref} - \frac{I_{Load2}}{C_{O2}} t \tag{32}$$

The voltage compensation by the buck converter can be calculated after running the achieved voltage and current equations for $N_{itr} = T_1/T_s$ iterations. Note that in the maximum voltage compensation, the C_{B2} reaches zero, the buck converter works in *CCM* mode to reach the steady state. On the other hand, t_{14} and t_{15} provide the required time for the buck's inductor current to reach zero before starting the next time interval. Thus, the initial conditions of the first iteration are given as below:

$$i_{L20} = 0 \tag{33}$$

$$V_{B20} = 0 \tag{34}$$

In the case of more than two channel power supplies, the buck converter should be able to regulate two or more channels at the same time. Since one series compensation circuit should be turned off during the on-time interval of the associated output flyback, the others are compensating the corresponding output voltage drop. The proposed high-frequency time-sharing operation technique in [18], is adopted in this paper for the control of the SIMO buck converter. For instance, in a three channel power supply if the first channel is being regulated by the flyback converter, the second and third series compensation circuits are enabled by turning on Q_{B2} and Q_{B3} in a time-sharing manner over a switching period Ts. Thus, each compensation circuit is active for Ts during a period of 3Ts. However, the switching frequency of the SIMO buck converter is Fs (500 kHz), and the regulating frequency of each buck converter is Fs/3. In this technique, the buck converter should work in *DCM* operation to avoid cross regulation.

3.2. Time Interval 2 (To/N~2To/N)

In this time interval, the series buck converter compensates for channel 1 while the flyback converter regulates channel 2. The principle of operation of the proposed master–slave power supply during *T2* is similar to that during time interval *T1* with characteristic time spans t_{11}, t_{12}, t_{13}, t_{14} and t_{15}. As a result, the equations and timing scheme previously detailed for channel 1′s flyback converter and channel 2′s buck converter within *T1*, can be modified for *T2* which combines channel 2′s flyback converter and channel 1′s buck converter. By using channel 2′s circuit parameters, channel 1′s flyback converter equations can be modified for channel 2.

4. Circuit Design

To verify the proposed methodology, a 28 V input triple output power supply was designed and simulated using MATLAB/Simscape. The rated output voltages of the converters were 15 V, 18 V and 30 V and each channel was rated for 1 A. The voltage levels were adopted such that the SIMO power supply works in both buck/boost operations. The key parameters of the power supply circuit are presented in Table 1.

Table 1. Circuit Parameter.

Sym.	Parameters	Value	Sym.	Parameters	Value
F_s	Converters Freq.	500 kHz	C_{O2}	Chan. 2 main Cap.	45 µF
F_O	Isolation Freq.	25 kHz	C_{b2}	Chan. 2 slave Cap.	30 µF
V_{in}	DC input voltage	28 V	C_{O3}	Chan. 3 main Cap.	30 µF
R_S	Sense Resistance	0.1 Ω	C_{b3}	Chan. 3 slave Cap.	25 µF
L_m	Mag. inductance	6 µH	r_C	Capacitor ESR	1 mΩ
L	Leak. inductance	*0.2* µH	R_{L1}	Chan. 1 load	15 Ω
L_{Buck}	Buck inductance	2 µH	R_{L2}	Chan. 2 load	18 Ω
C_{O1}	Chan. 1 main Cap.	50 µF	R_{L3}	Chan. 3 load	30 Ω
C_{b1}	Chan. 1 slave Cap.	30 µF	a1	Trans. turn ratio	1
			a2	Trans. turn ratio	1/30

Higher converter switching frequency is favorable with regards to limiting the output ripple voltage; however, due to practical limitations and trade off with efficiency it was set to 500 kHz. Output ripple voltage can be expressed as:

$$V_{Ripple} = \frac{r_C a D V_{in}}{F_s L_m} \tag{35}$$

where rc represents ESR of the filter capacitors. Proper selection of output frequency depends on the loads characteristics and provides enough time to regulate each channel during Tn. Based on the loads characteristics in this study, FO was selected such that the master converter regulates each channel within seven switching cycles.

$$T_1 \approx \frac{F_s}{3F_o}.\frac{1}{F_s} = \frac{500}{75}.T_s \approx 7T_s \tag{36}$$

In the power supply configuration without series compensation, the filter capacitor of the third channel for 1% load regulation is as high as 88 uF. While with the series compensation, 30 μF is enough.

$$C_{o1} = \left(\frac{2}{3}\right)\left(\frac{1}{25e3 \times 0.01 \times 30}\right) = 88\mu F \tag{37}$$

The magnetizing inductance of the flyback transformer was designed based on the minimum output voltage to ensure CCM operation for all channels which benefits from

smooth output voltage with lower spikes. The minimum Lm for boundary CCM/DCM operation of the channel with minimum voltage is given below [19]:

$$L_{m(min)} = \frac{a^2 V_o (1 - D_{min})^2}{2F_s I_O} = \frac{15(1 - 0.39)^2}{2 \times 500e3 \times 1} = 5.6\mu H \quad (38)$$

By assuming 5% input voltage variation for line regulation and 80% efficiency, Dmin is given below:

$$D_{min} = \frac{aM_{VDCmin}}{aM_{VDCmin} + \eta} = \frac{0.51}{0.51 + 0.8} = 0.39 \quad (39)$$

In order to mitigate cross regulation in high-frequency time-sharing operation technique [18], the buck converter inductor was set to 2 µH to achieve DCM operation. Simulation results in the next section show that with a 30 μF buck filter capacitor, 1% voltage regulation is achieved.

4.1. Flyback Converter Control Circuit Design

The simplified closed loop model of the flyback converter with peak current mode control is shown in Figure 10. Relative to voltage mode control, peak current mode control has faster transient response and higher gain bandwidth. These characteristics are crucial for the adopted time multiplexing switching scheme. However, if the duty cycle is greater than 50%, a perturbation in the current would cause a dramatic change in the duty cycle and lead to instability. To address the instability problem, a corrective ramp slope of Se was added to the current-sense signal (Sn). When the sum of these two signals exceeds the compensated signal Vc, the comparator turns off Qn. The compensation Se is a sawtooth ramp which should have a slope between 50 and 100% of the down-slope of Sn [21].

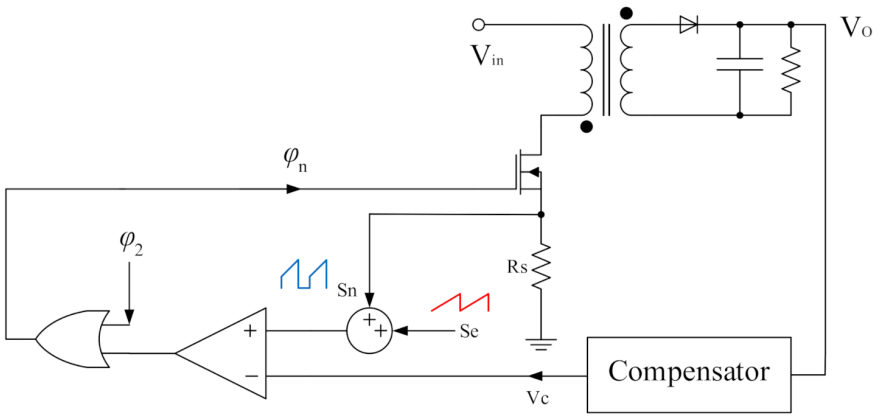

Figure 10. Simplified closed loop model of the flyback converter for the first channel.

In this section, the control loop design is conducted for the third channel. Since the duty ratio is always greater than 50%, the procedure can be easily extended to the first and the second channels. The inductor current ramp slope (S_n) is sensed by R_s once Q_n is turned on, which is computed as below:

$$S_n = \frac{V_{in}}{L_m}.R_s = \frac{28}{6\mu} \times 0.1 = 466\frac{mV}{\mu s} \quad (40)$$

According to [22], S_e is given below:

$$S_e = \left[\left(\left(\frac{1}{\pi} + 0.5\right).\frac{1}{1 - D}\right) - 1\right].S_n = 0.7S_n \quad (41)$$

In order to design the compensator, the overall transfer function of the flyback converter for *CCM* without the compensator is given below [23]:

$$F = A_{DC}.\frac{(1 + SC_o r_c).\left(1 - \frac{SL_m D}{R_L(1-D)^2}\right)}{\left(1 + \frac{SC_o R_L}{1-D}\right)\left(1 + S\frac{(1-D)\left(1+\frac{S_e}{S_n}\right)-0.5}{F_s} + \left(\frac{S}{\pi F_s}\right)^2\right)} \tag{42}$$

where A_{DC} is the DC gain of the power stage:

$$A_{DC} = V_{in}.\left(\frac{R_L}{R_S}\right).\left(\frac{1-D}{1+D}\right).\left(\frac{F_s}{S_n + S_e}\right) \tag{43}$$

Based on the above expressions, the overall transfer function can be simplified as below:

$$F = 1517\frac{(1 + S \times 3e - 8)(1 - S \times 5.58e - 7)}{(1 + S \times 0.002)(1 + S \times 5.15e - 7 + S^2 \times 4e - 13)} \tag{44}$$

The Bode plot of channel 3 is presented in Figure 11, which shows a negative phase margin. Therefore, the flyback converter is unstable and the control circuit should be compensated to achieve a stable and robust converter.

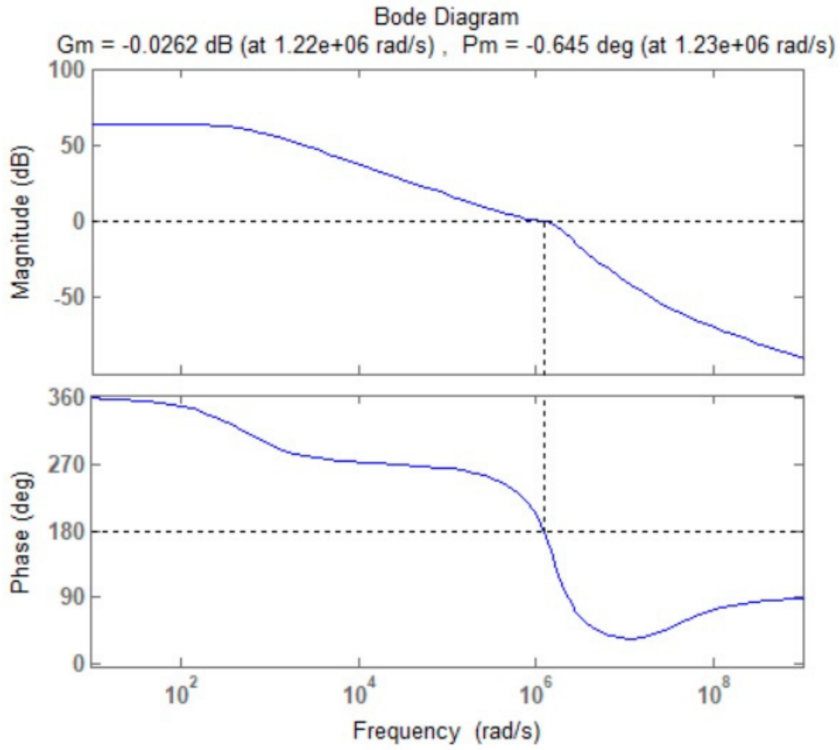

Figure 11. Bode diagram of channel 3 without compensator.

4.2. Compensator Parameter Selection

The type two compensation network in Figure 12 improves the overall system stability and guarantees zero steady state error by adding a pole at the origin for the compensator gain. Selection of compensator parameters should be started with the crossover frequency (Fo). For a current mode flyback converter, it should be well below right-half-plane (RHP) zero to attain high bandwidth while limiting the gain at high frequency [23]. The crossover frequency was selected as 5 kHz with respect to switching frequency to let the inductor store energy during t_{on} before it feeds the output capacitor during t_{off}. Thus, in case of a

sudden load change, the current in the inductor grows cycle by cycle at a sufficient pace to keep up with the demand.

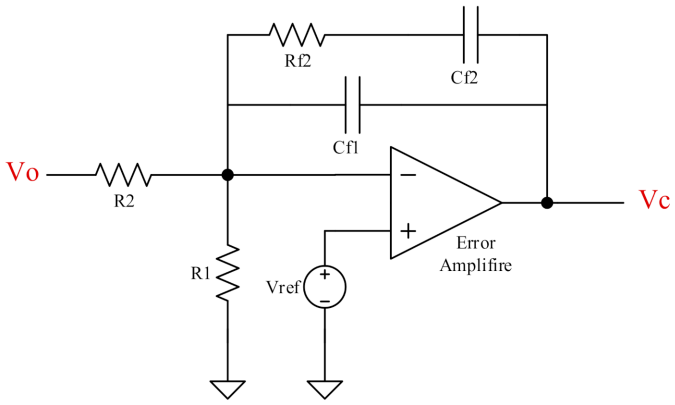

Figure 12. Type two compensation network.

Based on the gain margin in Figure 11, the "K Factor" method was used to attain a 90-degree phase margin and about 5 kHz bandwidth.

Given that the initial phase margin is −0.645 degrees and as it aimed to achieve a 90-degree phase margin, therefore the required phase boost is 90.645 degrees. A gain margin of 10 dB is reasonable, which allows the loop gain change by a factor of approximately three before the system becomes unstable [23]. In this research, the compensation network gain (G_M) was set to 25 dB to have a robust and stable system. Other parameters of the compensator can be achieved from the following steps [24]:

$$K = \tan\left[\left(\frac{\varphi_{boost}}{2}\right) + 45^o\right] = 116.73 \tag{45}$$

R_1 is a user selected variable and was chosen as 153 kΩ, in return R_2 is given as below assuming that Vref is 10 V:

$$R_2 = \frac{V_{ref} R_1}{\left(V_{in} - V_{ref}\right)} = 306k\Omega \tag{46}$$

$$R_{F2} = \frac{R_2 K^2}{G_M(K^2 - 1)} = 12k\Omega \tag{47}$$

$$C_{F1} = \frac{G_M}{K2\pi f_C R_2} = 0.03nF \tag{48}$$

$$C_{F2} = \frac{(K^2 - 1)G_M}{K2\pi f_C R_2} = 0.32uF \tag{49}$$

The transfer function of the compensation stage F_{Comp} (S) is found to be:

$$F_{comp} = -10 \times \frac{\left(1 + \frac{S}{247}\right)}{S\left(1 + \frac{S}{2.68e6}\right)} \tag{50}$$

Multiplying the compensation transfer function Equation (50) and the control to output transfer function Equation (44) gives the overall closed loop transfer function.

Figure 13 shows the bode diagram of the system closed loop transfer function. The compensated system has a 27.7 dB gain margin and an 88-degree phase margin.

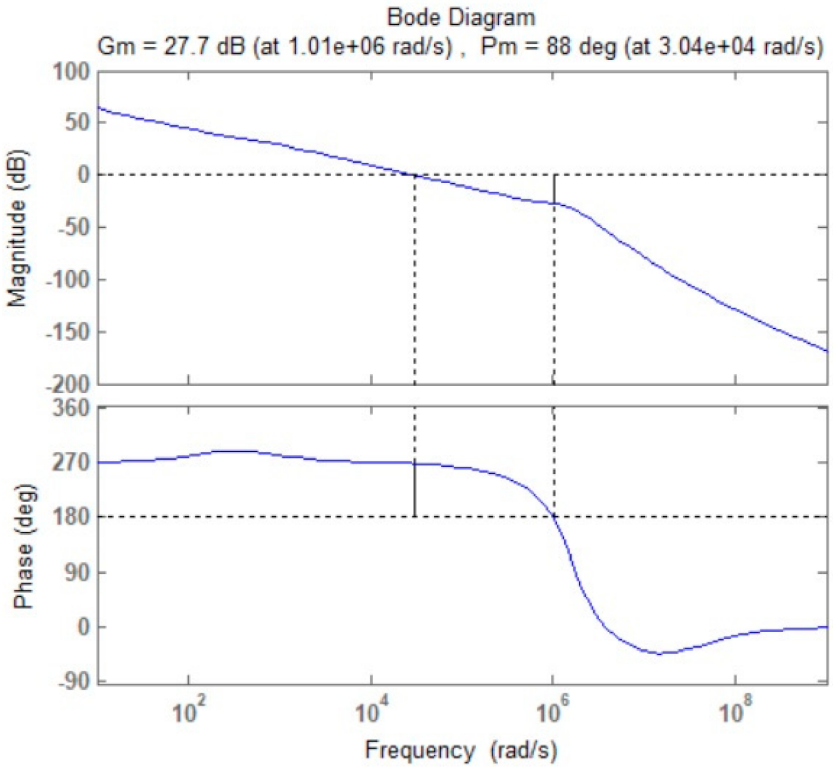

Figure 13. Bode diagram of channel 3 with type two compensator.

5. Simulation Results

Figure 14 depicts the simulation model of the proposed power supply in MATLAB/Simscape and Figure 15 shows channel 1 in detail. To protect Q_n during turn-off, an energy regenerative snubber is used to gracefully handle the high voltage spikes caused by leakage inductance. In the model, *Lr* is shown as the tertiary winding of the flyback transformer, while in practice it can be substituted with a fixed inductor to use the same number of components as a resistor–capacitor–diode (*RCD*) snubber circuit and decrease the overall form factor.

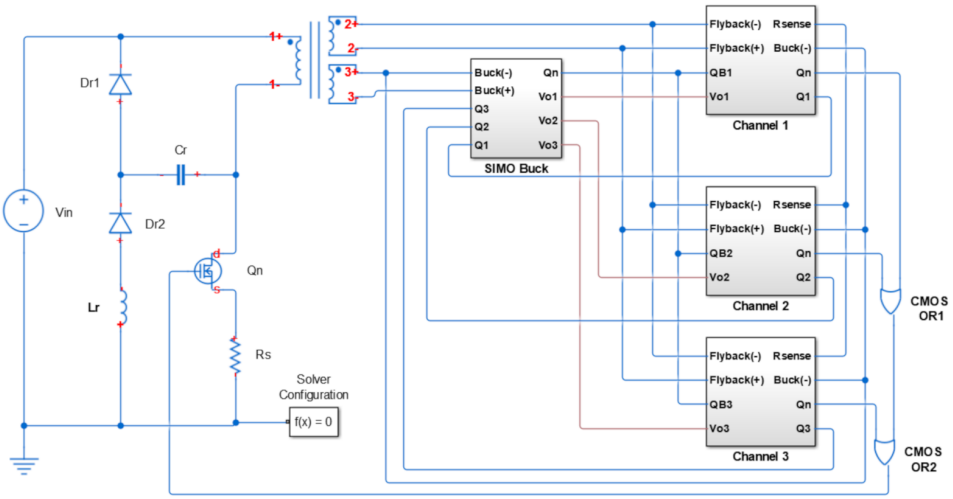

Figure 14. Block diagram of the proposed converter as a three-channel power supply.

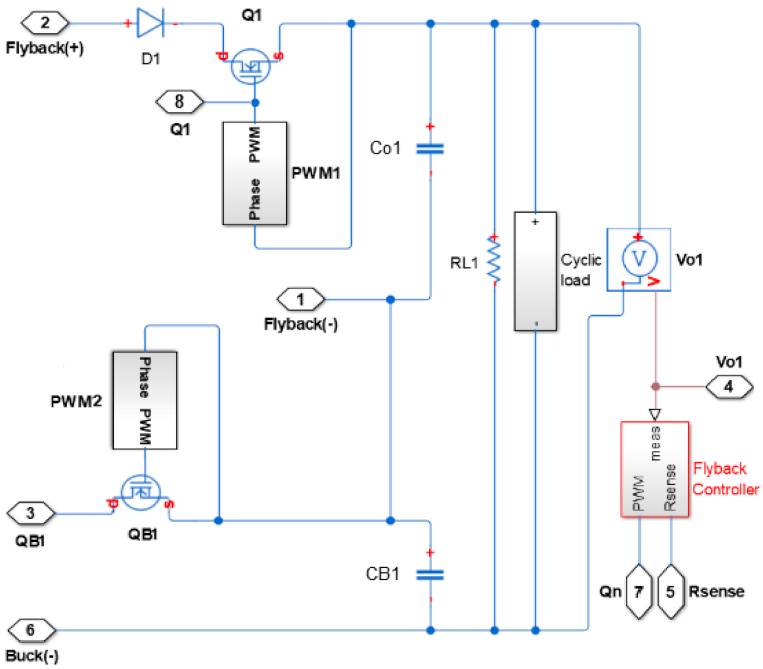

Figure 15. Expanded view of channel 1 showed in Figure 14.

A controlled dc current is placed in parallel with the constant load in the model in Figure 15 to implement 20% load change and study the load regulation of proposed power supply. While the duty cycle of Q_1 for a three-channel power supply is about one third, the duty cycle of Q_{B1} is about two thirds to provide complete series voltage compensation.

In Figure 16, a synchronous buck converter is depicted which is fed by the flyback converter. The input capacitors of the buck converter (C_{S1}, C_{S2}, C_{S3}) have been charged alternatively while the associated switch (Q_{S1}, Q_{S2}, Q_{S3}) is turned on simultaneously with the corresponding flyback isolating switch (Q_1, Q_2, Q_3). The proposed topology maintains a nearly constant voltage at the input of the buck converter with the flyback converter inducing different voltage values during T_1, T_2 and T_3. The size of input capacitors should be calculated as below to attain the aforementioned goal:

$$V_{C_{S1}} + V_{C_{S2}} + V_{C_{S3}} = 1V \tag{51}$$

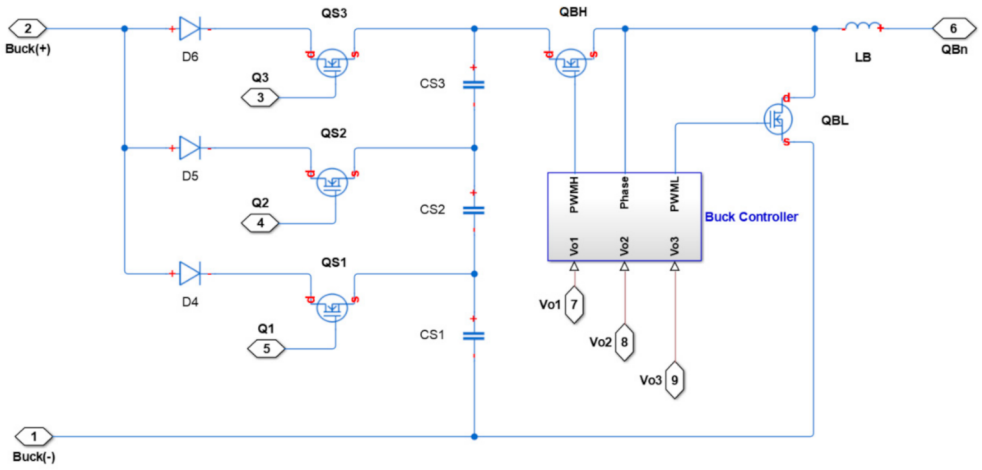

Figure 16. Expanded view of SIMO buck converter showed in Figure 14.

Assuming the highest output voltage is 30 V, *a2* should be one thirtieth of *a1* to receive utmost 1 V from the tertiary winding. It yields:

$$V_{C_{S1}} = \frac{15}{30} = 0.5V \tag{52}$$

$$V_{C_{S1}} + V_{C_{S2}} = \frac{18}{30} = 0.6V \tag{53}$$

As a result, the relation between input filter capacitors of converter is given as below:

$$C_{S2} = 5C_{S1} = 4C_{S3} \tag{54}$$

According to Equation (54) and to maintain 5% input voltage variation, the buck's input capacitors are set as follows:

$$C_{S1} = 4 \text{ uF}$$

$$C_{S2} = 20 \text{ uF}$$

$$C_{S3} = 5\ uF$$

Start-up and steady state response of the power supply to 1 A load is illustrated in Figure 17. The output voltages are maintained within 1% of the rated value, while the filter capacitors are sized as half of the capacitor in the converter without series compensation. The output voltages at steady-state are (14.91–15.14 V), (17.89–18.16 V) and (29.72–30.24 V) for channels 1, 2 and 3, respectively. Operations of the main and the slave converters can be distinguished in the close-up view of Figure 17. The leakage inductance of flyback transformer causes thicker and steeper regulating current, and operation of the buck converter corresponds to smoother lines.

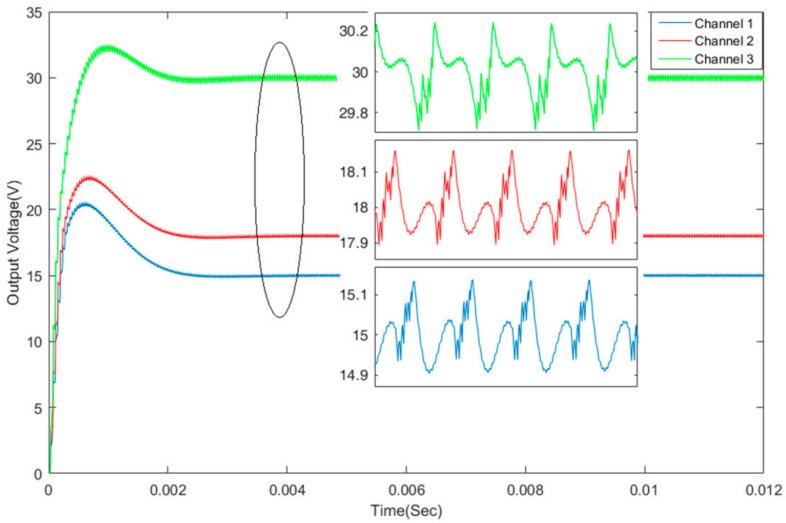

Figure 17. Start-up and steady state response of the proposed power supply associated with channel output voltages.

Figure 18 shows that the proposed topology for the SIMO buck converter maintains input voltage within 5% of the rated value. The summation of input capacitors' (C_{S1}, C_{S2} and C_{S3}) voltage supplies the buck converter which stands in the range of 0.9524–1.039 V. While C_{S1} is charged during the on-time intervals of all flyback channels, C_{S2} is charged during T_2 and T_3, and C_{S3} is charged just during T_3. As a result, C_{S1} reflects the minimum voltage deviation in the Figure 18 and C_{S3} the maximum.

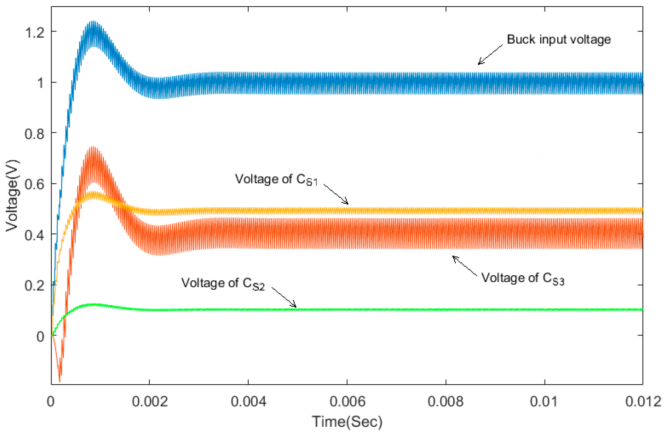

Figure 18. Input voltage of SIMO buck converter in terms of input filter capacitors.

Figure 19 reveals that about 0.7662 V is inserted into the output voltage by the series compensation of the first channel, and this keeps the load voltage regulated within 1%. More importantly, the inserted series voltage drops to about zero during turn-OFF time intervals of the buck converter and lets the output channel receive maximum voltage compensation during turn-OFF time intervals of the flyback converter. While according to Equation (3) channel 1 is expected to receive the highest series compensation due to lower output voltage, its relatively larger flyback converter filter capacitor takes over a greater portion of regulation and consequently the associated buck converter adapts the inserted series voltage to a lower value. On the other hand, the highest inserted series voltage of 0.9248 V was received by the third channel which has the least voltage compensation requirement and the highest output voltage.

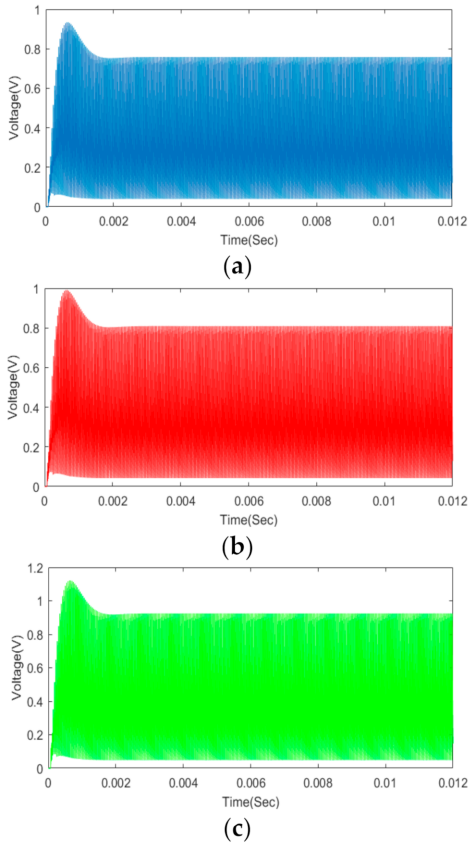

Figure 19. Output voltage of buck converter (**a**) channel 1 (**b**) channel 2 (**c**) channel 3.

The demand for a higher series compensation from the third channel buck converter is due to the use of a relatively small capacitor on the flyback converter. The series compensation received by the first, second and third channels is in an ascending order of magnitude. Specifically, the steady state root-mean-squared (RMS) voltage values of the buck converter are VOB1 = 0.4221 V, VOB2 = 0.4456 V and VOB3 = 0.5634 V.

Figure 20 shows transient response of converter to the change of load which is applied via the controlled dc current as 100 mA for $t \in [0, 0.006]$ and -100 mA for $t \in [0.006, 0.012]$. In response to a $\pm 10\%$ load change the output voltages are maintained within 4% of the rated value as (14.46–15.61 V), (17.42–18.68 V) and (29.17–30.92 V), and return to 1% regulation after 2.3 m/s, 2.2 m/s and 1.8 m/s, respectively. Robust stability of the proposed power supply is demonstrated in Figure 20 by limiting undershoot and overshoot corresponding to the load change to 4.06%, 3.78% and 3.06% for first, second and third channels, respectively.

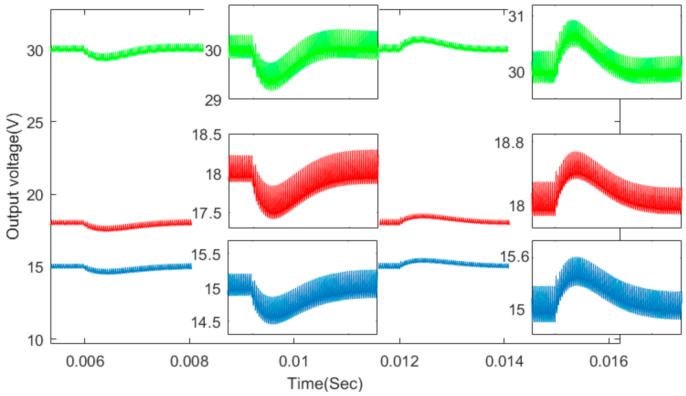

Figure 20. Channels' output voltage of the proposed power supply in response to a $\pm 10\%$ load change.

The steady state output currents of the buck converter are depicted in Figure 21. They oscillate between 1.5 A and -1 A in which the lower range is the rated current of the load and is drawn during turn-OFF intervals of series compensation, and series compensation regulating current which is about 1.5 A.

The maximum output current I_{OB1} = 1.461 A, I_{OB2} = 1.519 A and I_{OB3} = 1.611 A and its RMS values are I_{OB1} = 0.8940 A, I_{OB2} = 0.8960 A, I_{OB3} = 0.8962 A. The ratio of the first channel buck converter's input power to its rated power is as derived below:

$$\frac{P_{B1}}{P_{O1}} \approx \frac{V_{OB1(rms)} I_{OB1(rms)}}{V_{O1} I_{O1}} = \frac{0.8940 \times 0.4221}{15 \times 1} \approx \frac{1}{40} \tag{55}$$

Similarly, the ratios for the second and third channels which are less than the first channel is expressed as:

$$\frac{P_{B2}}{P_{O2}} \approx \frac{V_{OB2(rms)} I_{OB2(rms)}}{V_{O2} I_{O2}} = \frac{0.8960 \times 0.4456}{18 \times 1} \approx \frac{1}{45} \tag{56}$$

$$\frac{P_{B3}}{P_{O3}} \approx \frac{V_{OB3(rms)} I_{OB3(rms)}}{V_{O3} I_{O3}} = \frac{0.8962 \times 0.5634}{30 \times 1} \approx \frac{1}{60} \tag{57}$$

The total power consumed by the buck converters expressed as a ratio of the rated power of the converter is:

$$\frac{P_{B(Total)}}{P_{O(Total)}} = \sum_{n=1}^{3} \frac{V_{OBn} I_{OBn}}{V_{On} I_{On}} = \frac{2.34}{63} \approx \frac{1}{50} \tag{58}$$

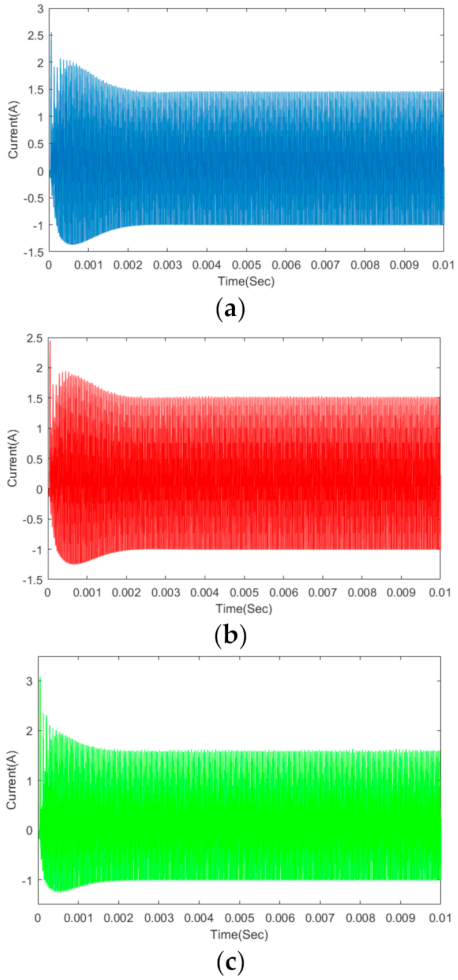

Figure 21. Steady state output current of the buck converter (**a**) first channel (**b**) second channel (**c**) third channel.

Due to the low-power low-voltage circuit of the series compensator, it is practical to implement all buck converters' components integrated on-chip and as a result the slave converter would not change significantly the overall form factor of the power supply. Table 2 represents a comparative analysis of the proposed SIMO converter with similar published research works [13,25–28]. As per Table 2, the previous works have been provided so that the table it covers a range of very low-power to middle-power topologies and they can be adopted for non-isolated application. However, the proposed SIMO converter falls into the low-power class and is capable of working in boost/buck mode and is suitable for the applications for which isolation is required. From tabular data in Table 2, it can be seen that [26–28], provide a better output voltage ripple; however, it is either because of a low load current or large adopted output capacitor. In [27,28], 10 uF output capacitors are relatively designed to be large with respect to the 45 m/A load current. Although average load current in [26], is 1.5 A and is comparable to the 1 A load current in the proposed converter, its output capacitor is nine times bigger. The adopted low-power series buck converter compensates for the output voltage deviation such that output voltage ripple stays within 1% of rated value. Another criterion that consistently is being compared in the research literature, is the number of power switches. From the efficiency point of view, the switching power loss in both noncontrollable (Diodes) and controllable power switches results in poor efficiency and the number of both kinds of power switch should be taken into account. In the proposed converter, a total of five high power switches including the power diodes, have been incorporated into the master converter. Note that the switching

frequency of Q1 and Q2 is 1/20 of the converter switching frequency which means that the contribution of Q1 and Q2 to the switching power loss is not as much as other switches.

Table 2. Comparison among SIMO DC converters normalized for two output channels.

Parameter	[13]	[25]	[26]	[27]	[28]	Proposed Converter
Vin	12 V	18 V	48 V	3.7 V	2.5 V	28 V
Vo	V_1: 28 V, V_2: 200 V	V_1: 12 V, V_2: 8 V	V_1: 12 V, V_2: 60 V	V_1: 1 V, V_2: 1.8 V	V_1: 3.4 V, V_2: 1.8 V	V_1: 15 V, V_2: 30 V
Ptotal	635 W	33 W	79 W	0.168 W	0.326 W	45 W
Max. Co	100 uF	220 uF	470 uF	10 uF	10 uF	50 uF
L	75 uH	100 uH	5 mH	4 uH	4.7 uH	6 uH
Vo Ripple	-	4%	0.1%	0.58%	0.8%	0.93%
Buck/Boost mode	No	No	Yes	Yes	Yes	Yes
Isolated	No	No	No	No	No	Yes
Power Switch	1	3	1	6	5	3
Power Diode	4	1	2	0	0	2

6. Conclusions

A novel multiple channel power supply based on master/slave topology is proposed in this paper. The power supply configuration is achieved by adding a SIMO buck converter, as slave converter, in series to master flyback converter. The switching scheme employed in the power supply makes use of just one three-winding transformer sufficient for a triple output converter. This scheme achieved independent channel output control, resolves cross regulation, reduces flyback filter capacitor size and converter footprint, ensures tight regulation and fast transient response. Mathematical models were used to carry out thorough transient and steady state analysis on the converter. The power and control stages of a triple output power supply were designed to target tight regulation, robust stability and fast transient response and its performance is verified with MATLAB/Simscape. Moreover, with a flyback capacitor size less than half of that in conventional topologies, a regulation error less than 1% is achieved. The simulation also demonstrates fast recovery and small overshoot/undershoot after a load change of ±10% with output voltage staying within 4% of the rated value. With all the desired performances, the slave converter does not have a meaningful negative impact on the efficiency of the proposed power supply circuit due to its low voltage rate (<1 V) and low power consumption, which is about 1/50 of the flyback converter power consumption on average. The limitation of the flyback converter in low-power applications is because of the way that energy is stored and transferred via the air gap in the SMPS transformer. In the next step, the series voltage compensation will be adopted in forward or push–pull converters to develop a SIMO converter for mid-power applications.

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