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A High-Efficiency and Wide-Input Range RF Energy Harvester Using Multiple Rectenna and Adaptive Matching [†]

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Abstract: In this paper, a Radio Frequency (RF) energy harvester (EH) system for Internet of Things (IoT)-related applications is presented. The proposed EH architecture operates at 5.2 GHz band and utilizes multiple rectenna. This approach enhances the efficiency of the whole system over a wide dynamic RF input range. In the presented circuit, configuration of the rectenna is controlled by Field-Programmable Gate Array (FPGA) with respect to the input power level of the received RF input signal. In addition, an automatic adaptive matching based on the configuration of the rectenna, level of the received signal, and load current adjusts the matching network. The rectenna is realized through the Radio Frequency-Direct Current (RF-DC) converter composed of two Schottky diodes and generates the output DC voltage. Finally, a buck-boost converter provides the flattened and fixed voltage for the IoT and wearable devices. The 5.2 GHz band reconfigurable system demonstrates 67% high efficiency and 6.1 V output DC voltage where the power level of RF input is +20 dBm. The main application of the proposed structure is for charging wearable smart devices such as a smart watch and bracelet.

Keywords: RF energy harvester; power conversion efficiency; rectenna; IoT/wearable devices; adaptive matching; wide input range

1. Introduction

Nowadays, the Internet-of-Things (IoT) and Bluetooth low-energy (BLE) devices have made a smart environment by using wireless sensors and communication protocols. These technologies transmit data for making decisions related human issues, health cares, and automation of the facilities. Communication without any interruptions and long battery life are the most challenging requirements for these aims. Wireless sensors need continuous power, which, with the conventional methods, suffer from the short lifetime of the batteries. In addition, an energy harvester (EH) and low-power devices may not be installed under normal conditions, and their batteries cannot be changed easily [1,2].

Longer battery life and a system with no need to recharge demands a low-power and high-efficiency power management-integrated circuit (PMIC). In addition, chip area and external passive components such as inductors and capacitors are other design challenges. Generally, parasitic elements, printed circuit boards (PCBs), and line losses are the targets of improvements, while recent trends have focused on the integration of an energy harvester power management system, especially an Radio Frequency (RF) EH system with an IoT/wearable or RF transceiver system [3,4].

Due to problems associated with the replacement or recharging of batteries, self-powering based on an energy harvesting communication network is a critical demand for these wireless devices. The main focus of recent work is remote charging via an EH from a renewable source and optimizing the processing methods [1–8]. Besides thermal, solar, and wind energy sources for EH, recently, the presence of ambient radio frequency (RF) signals is becoming an appealing source for EH in portable devices. The capability of the RF signals in carrying information in wireless devices introduces the concept of simultaneous wireless information and power transfer (SWIPT). SWIPT offers a noticeable concept in the field of communication systems, which provides efficient energy and information transfer in addition to powering an RF EH system.

Figure 1 shows the top block diagram of an RF EH system for IoT/wearable applications. The antenna, rectifier, DC-DC converter, and load are the main building blocks of an RF EH system. The overall efficiency of the whole system is determined by the RF-to-DC and DC-DC converter efficiency. Based on the received power and converted DC voltage level, buck or boost modes would be selected. Providing a higher output DC voltage and using a simple highly efficient buck converter are preferable in comparison to a buck-boost converter. In contrast, enhancing the RF EH system overall efficiency requires the design of a high-output DC voltage rectifier with high power conversion efficiency (PCE).

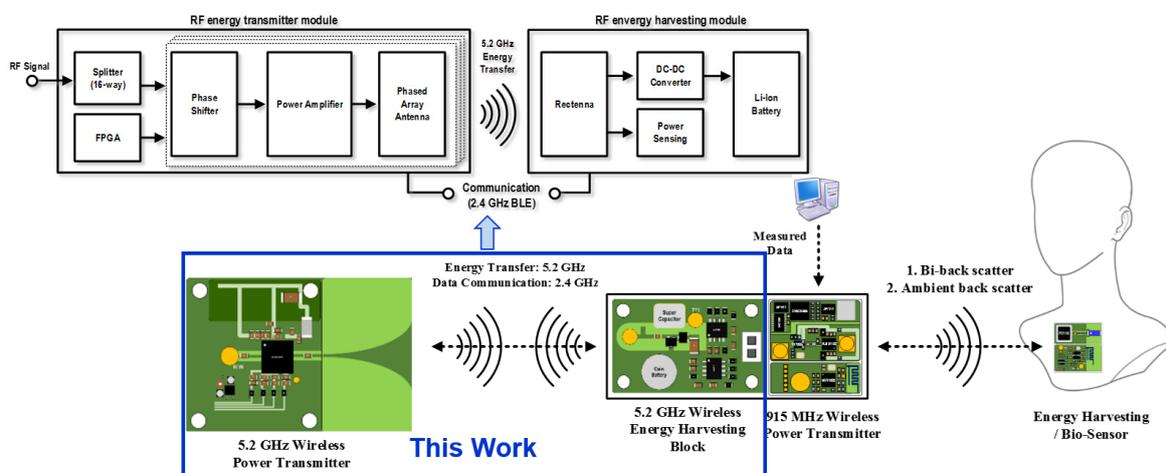


Figure 1. Top block diagram of the radio frequency (RF) energy harvester. Reprint with permission [4775431338148]; 2020, IEEE.

This paper is organized as follows: The top system architecture and detailed building blocks of the proposed RF EH system are described in Section 2. Section 3 focuses on the implementation and experimental result. Section 4 concludes the paper.

2. Architectural and Detailed Building Blocks of the EF EH System

2.1. Architecture

Figure 2 indicates the system budget and path loss measurement vs. the distance of the RF EH system. The maximum available power at the Receiver (Rx) antenna is given by

$$P_R = P_T + G_T + G_R - \text{Path loss} \quad (1)$$

where, in the Tx module, P_T and G_T are the respective output power and antenna gain, and in the Rx module, G_R and P_R are the respective antenna gain and received power. Path loss is the air loss of the measured environment. Table 1 demonstrates the system budget considering an ideal system structure, the distance between Tx and Rx modules, and the free space path loss (FSPL) equation. To maximize the RF power level for RF-DC conversion and eliminate the air here, a 6-array antenna is designed. An automatically adapted and reconfigurable multiple rectenna architecture depending on the RF input signal level is presented.

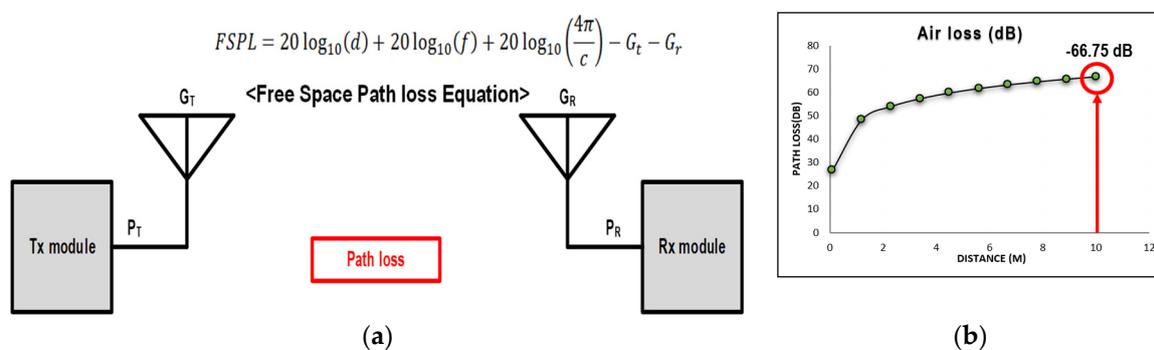


Figure 2. (a) System budget and (b) path loss measurement vs. distance. Reprint with permission [4775431338148]; 2020, IEEE.

Table 1. System Budget. Reprint with permission [4775431338148]; 2020, IEEE.

Distance (m)	Output Power (P_T) (dBm)	Transmitter Antenna Gain (G_T) (dBi)	Receiver Antenna Gain (G_R) (dBi)	Path Loss (dB)	Received Power (dBm)
10				-66.75	0.967
5	48	7.317	13 (6 array rectenna)	-60.73	6.987
1				-46.75	21.067

Figure 3 illustrates a block diagram of the proposed RF EH system [8]. It comprises a 2×3 array patch antenna, 6-parallel RF-DC converter in the front side, DC-DC converter, BLE module, and Universal Serial Bus (USB) connector on the back side of the Rx module PCB board. The front view of the PCB has a rectenna composed of five RF-DC converters and five patch antennas; one RF-DC converter and one patch antenna are configured for the pilot signal only. The proposed RF-DC converter of each rectenna is fabricated based on a Dickson charge pump structure. A six-array rectenna with two Schottky diodes was adopted to produce high efficiency and high-output DC voltage. It has an optimized third harmonic source termination for an improved conversion efficiency, and the implemented RF-DC converter includes series transmission lines and open-stubs for the third harmonic inductive termination and fundamental impedance matching. The simulated third harmonic contour using the harmonic source-pull simulation shows an optimum region near $jX75 \Omega$ with a maximum efficiency of 69.45%. The optimum third harmonic impedance is inductive due to the junction capacitance of the Schottky diodes, and the input capacitance and inductive source impedance produce parallel

resonance for an appropriate Class-F third harmonic termination. Compared to the efficiency of the rectifier without harmonic control, the proposed rectifier with harmonic control exhibits a 5.2% higher efficiency at an input power of about +20 dBm. Using the optimum third harmonic termination, the voltage waveforms across the Schottky diodes of RF-DC converters become closer to the square waves of an ideal RF-DC converter. The rectenna is the first block at the input of the Rx module to rectify the RF signal. A combining capacitor at the output of the rectenna is also used as a low-pass filter to remove ripples at the output. The output of the rectenna is fed to the buck-boost converter. In order to eliminate voltage variation, a buck-boost converter is used to produce constant output voltage. When the input voltage level reduces due to the weak RF signals, the boosting operation of the buck-boost converter is performed to maintain the output voltage level and vice-versa. A low drop-out (LDO) regulator can be used to maintain a constant output voltage. A super capacitor is connected at the output of the buck-boost converter to store energy and provides power for IoT/wearable devices and charging the battery.

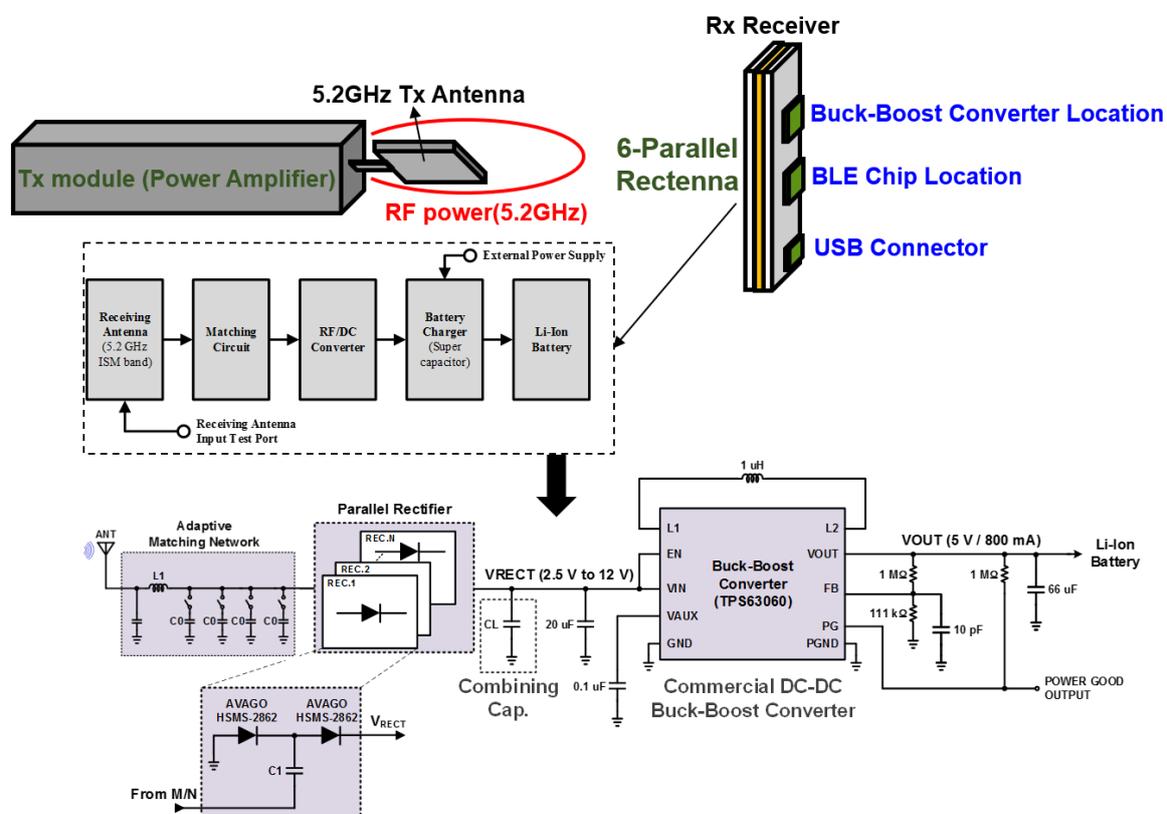


Figure 3. The proposed RF energy harvester system block diagram. Reprint with permission [4775431338148]; 2020, IEEE.

The front and back sides of the EH system are implemented using RF-35 and FR4 with four layers through the commercial components to maximize the board efficiency. The multiple rectenna configuration is automatically selected with respect to the input power level. The sensitivity and input range of the RF EH system are from 0 dBm to +30 dBm, while the peak power efficiency is 67% when the received RF input power level considering the air loss is +20 dBm at 5.2 GHz. The RF EH system charges the IoT/wearable devices at a distance of 78 cm with a single 5.2 GHz Tx antenna charging station with a 1 W transmit power and a distance of 5.5 m with a 48-array antenna charging station with 3.6 W transmit power [9].

2.2. Reconfigurable Rectenna

The nonlinear behavior of the antenna and transistor in both the on and saturation regions determines the saturation effects, while the efficiency of the SWIPT decreases when the RF input signal level exceeds a certain value. The reconfigurable parallel rectenna eliminates the saturation nonlinearity. This reconfigurable approach using rectenna to split the RF input power of the RF-DC converter among parallel rectennas (antennas, and RF-DC converters) ensures its reliable operation beyond the saturation region [10].

The proposed N_{EH} (Number of rectenna circuits) multiple rectenna basic structure is depicted in Figure 4. The RF-DC circuits can be implemented in parallel and series to maximize the efficiency of the system. The RF-DC circuits in this work are implemented in parallel and are followed by a DC combiner capacitor to limit the complexity of the system. The nonlinear EH is reconfigured adaptively based on the received signal power and is controlled by FPGA. An identical nonlinear EH model for each rectenna, especially the RF-DC circuit, is assumed [11–13]. Hence, the harvested power of the i th rectenna circuit, denoted by $P_{EH,i}$, is expressed as

$$P_{EH,i}(\alpha, P_R) = \alpha \frac{P_{sat}(1 - e^{-c_1 P_R})}{1 + e^{-c_1(P_R - c_0)}} \quad (2)$$

where $P_{EH,i}$ is the RF EH power and P_{sat} is the maximum RF EH power due to device saturation. α is the receive mode indicator variable being set to 1 to obtain the maximum power, and P_R is the receive power. Here, c_0 and c_1 are the constants related to the specifications and shape of the input signal in the energy harvesting circuit.

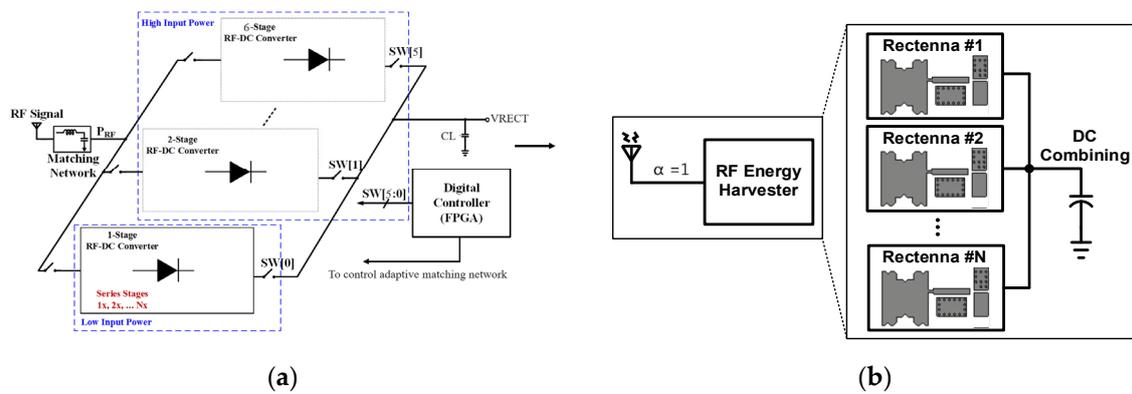


Figure 4. (a) The proposed rectenna structure and (b) Its parallel configuration. Reprint with permission [4775431338148]; 2020, IEEE.

All the received signals from antennas are fed to the EH when $\alpha = 1$ and then split evenly among N_{EH} (#of RF-DC circuits) multiple rectenna circuits. We assume an ideal EH with no energy loss in energy conversion from parallel rectenna circuits to the DC combining capacitor and during power splitting. With the assumption of an ideal EH, the harvested power at the DC combining capacitor is linearly increased to

$$P_{EH,total} = \sum_{i=1}^{N_{EH}} P_{EH,i}(\rho_i P_R) \quad (3)$$

where ρ_i is the power-splitting ratio for the i th rectenna circuit. As each rectenna circuit is modeled by the identical nonlinear function with $\rho_i = 1/N_{EH}$ and $P_{EH,i} = P_{EH,1}$ for $\forall i$, the total harvested power becomes

$$P_{EH,total} = N_{EH} P_{EH,1} \left(\frac{P_R}{N_{EH}} \right) \quad (4)$$

For understanding the effect of the power-splitting ratio $\rho = [\rho_1, \rho_2, \dots, \rho_{N_{EH}}]$, consider an example with two rectennas in the simplest energy harvester system. In this case, drop the circuit index of the power-splitting ratio and simplify the total harvested power to

$$P_{EH,total}(\rho, P_R) = P_{EH,1}(\rho P_R) + P_{EH,1}[(1 - \rho)P_R] \quad (5)$$

where $\rho \in [0, 1]$. $P_{EH,total}$ varies as the received power P_R or the power-splitting ratio ρ changes. With fixed P_R , $P_{EH,total}$ can be maximized by optimizing ρ .

The optimal ratio ρ^* changes with the received signal power P_R . When P_R is low, only a single rectenna circuit is activated by controlling $\rho = 0$ or 1. For high P_R , we would better activate both rectenna circuits by splitting the received power evenly ($\rho = 0.5$). This is the direct consequence of the nonlinear behavior of the rectenna circuit. The EH efficiency becomes very low for low P_R , and thus, it is more appropriate to use a single rectenna circuit instead of both. For high P_R , using a single rectenna circuit causes saturation, and it is desired to activate both rectenna circuits. Splitting the received power evenly reduces the excess power due to the saturation. Based on these observations, the total harvested power can be expressed as

$$P_{EH,total} = \max \left\{ P_{EH,1}(P_R), 2P_{EH,1} \left(\frac{P_R}{2} \right) \right\} \quad (6)$$

With the increase in the number of rectenna circuits, the energy harvester can reconfigure in a similar way according to the received power with an even split. The total harvested power is $P_{EH,total} = N_{EH^*} P_{EH,1}(P_R/N_{EH^*})$, where N_{EH^*} is the number of activated rectenna circuits based on the received power. N_{EH^*} can be determined by $N_{EH^*} = \arg \max N_{EH} \{P_{EH,1}(P_R), \dots, N_{EH} P_{EH,1}(P_R/N_{EH})\}$, yielding the optimal power-splitting ratio $\rho_i^* = 1/N_{EH^*}$, $i \in \{1, \dots, N_{EH^*}\}$.

The reconfigurable EH with multiple rectenna circuits implemented in parallel at a high input power level always perform better than the EH with fixed multiple rectenna circuits.

Find the maximum power conversion efficiency (PCE) of the reconfigurable rectenna: The reconfigurable EH is proposed, where multiple rectenna circuits are implemented in parallel at a high input power level while being implemented in series at a low input power level. The reconfigurable EH certainly brings higher PCE than the EH with fixed multiple rectenna circuits.

Case I: High input signal power level ($P_R > P_{R, opt.}$)

In this case, we have to divide the high input power among multiple rectenna circuits in parallel such that

$$\frac{P_R}{N_{EH}} < P_{R, opt.} \quad (7)$$

where N_{EH} is the number of rectenna circuits depending on the received signal power. In this case, the rectenna design in parallel structure is preferred.

Case II: Low input signal power level ($P_R \ll P_{R, opt.}$)

In this case, we have to power-up the low input signal power level or use low V_{th} devices such that

$$P_R < P_{th, ON}. \quad (8)$$

The rectenna design in series structure can be a good candidate. In this paper, to prevent PCE degradation, the proposed structure can be made reconfigurable, which can be controlled by FPGA both in parallel and series. For example, in the parallel structure, to find the optimal value of N_{EH} based on the measurement performance of single rectenna circuit as shown in Figure 5, $P_{R, opt.}$ should be first determined. Then, based on the two conditions below, the optimum N_{EH} can be determined as follows:

$$\left\{ \begin{array}{l} \frac{P_R}{N_{EH}-1} > P_{R, opt.} \\ \frac{P_R}{N_{EH}} < P_{R, opt.} \end{array} \right. \quad (9)$$

Therefore, the PCE can be written as follows:

$$\eta = \sum_{i=1}^{N_{EH}} C_i N_{EH} f_i\left(\frac{P_R}{N_{EH}}\right) \tag{10}$$

$$\left\{ \begin{array}{l} f_i\left(\frac{P_R}{N_{EH}}\right) = f\left(\frac{P_R}{N_{EH}}\right) \forall i \\ C_i = C \text{ (coupling loss and constant)} \end{array} \right.$$

where C_i is the coupling loss factor proportional to the number of rectenna circuits (N_{EH}). C_i can slightly change the slope of the PCE curve and P_{sat} . As a result, the simplified optimization problem for maximum PCE over the two factors P_R and N_{EH} can be formulated as follows:

$$\eta (PCE) : \max_{N_{EH}} CN_{EH}f(x). \tag{11}$$

Based on the peak PCE of a single-stage rectenna and the above equation, we can determine the maximum $PCE = P_{sat} = f(x)$ for $x = \frac{P_{R, opt.}}{N_{EH}}$.

$$\eta (PCE) : \max_{N_{EH}} CN_{EH}f\left(\frac{P_{R, opt.}}{N_{EH}}\right); 0 < C \leq 1 \text{ and } C \propto N_{EH} \tag{12}$$

To obtain the optimal PCE, we first determine $f(x)$ that is proportional to $P_{R, opt.}$ and N_{EH} . N_{EH} can be determined by (9). Moreover, to find the coupling loss factor value, which is proportional to N_{EH} , the peak PCE of the single-stage rectenna in the measured point of view is needed. Similarly, the series structure can be described with the necessary changes.

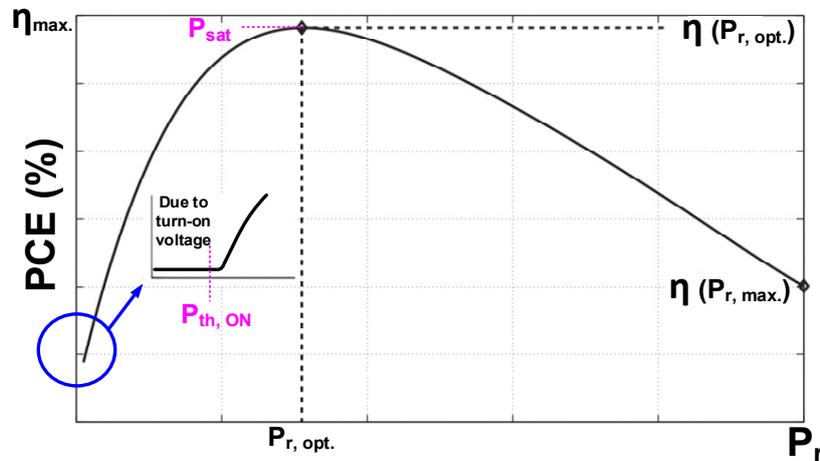


Figure 5. Non-linear PCE curve characteristics of the single-stage rectenna.

2.3. Tx and Rx Antenna Design

The antenna takes the RF signal (5.2 GHz) from the Tx power amplifier and feeds it to the EH system and memory cell. A Koch fractal patch antenna with high reflection co-efficiency and gain and an inter-element spacing equal to 0.5λ (at the design frequency of 5.2 GHz, λ is the wavelength in free space) as a compact size for the Rx module side is implemented as shown in Figure 6.

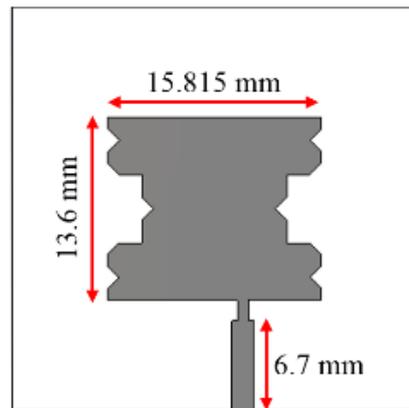


Figure 6. Koch fractal patch antenna. Reprint with permission [4775431338148]; 2020, IEEE.

Figure 7a,b illustrate a 5.2 GHz Quasi-Yagi antenna configuration on the substrate of Taconic RF-35 (0.76 mm) to transmit a total power of 3 W, being used as a wireless power transmitter and its specification.

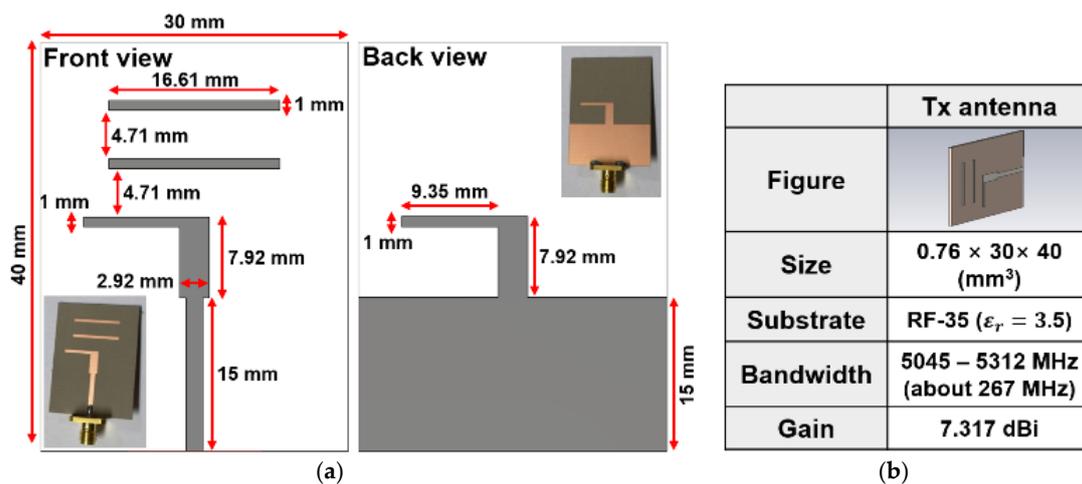


Figure 7. Configuration of the designed quasi-Yagi Tx antenna, (a) Front and back sides, (b) Specifications of the Tx antenna. Reprint with permission [4775431338148]; 2020, IEEE.

An Rx module designed by a 2 × 3 array antenna is located at a distance up to around 1 m (the distance can vary to harvest more RF input power) from the transmitter to harvest the transmitted power as shown in Figure 8a. The broadside gain of each port Rx antenna is shown in Figure 8b.

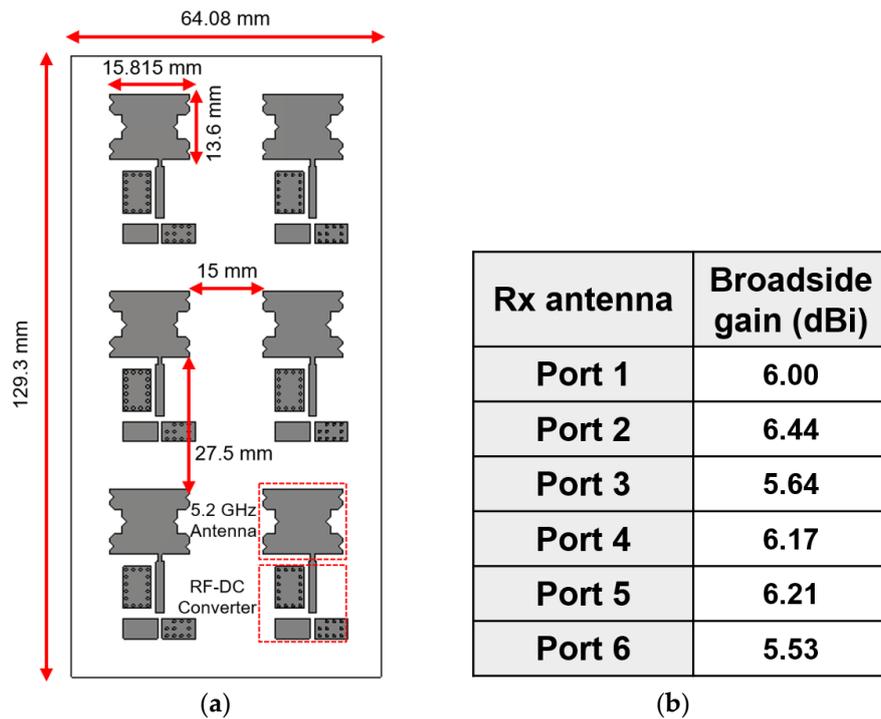


Figure 8. (a) 2×3 Rx module antenna arrangement and (b) Specifications. Reprint with permission [4775431338148]; 2020, IEEE.

3. Implementation and Experimental Results

The module of the proposed RF EH including reconfigurable scheme and third harmonic control with the information of the PCB layers is shown in Figure 9a,b. The 6-parallel rectenna shows 67% conversion efficiency and higher than 6.1 V output DC voltage at the input power level of +20 dBm. 4% improvement in efficiency is achieved in compared with the case without the third harmonic control circuit and efficiency.

The presented RF-DC converter simultaneously provides both higher output DC voltage and conversion efficiency, and this results in a higher overall conversion efficiency and simpler system configuration of the whole RF EH system. Figure 10a–c show measurement environments of RF EH systems. During the measurement in two setups, a 5.2 GHz RF signal via the power amplifier and Tx antenna is transmitted, which charges the wearable device, chip Light Emitting Diode (LED), mobile phone, and LG products at respective distances of 65 cm, 80 cm, 90 cm, and 25 cm, with a transmission power of 34.77 dBm for the wearable device, chip LED, and mobile phone and 30 dBm for LG products. Figure 11a,b show the measured reflection coefficient (S11) of Tx antenna and Rx antennas, respectively. The -10 dB reflection bandwidth of the designed Tx antenna is 7.4% (5.08–5.32 GHz). The measurement results for power conversion efficiency of the RF EH system are illustrated in Figure 12. The rectenna provides a maximum 6.1 V output DC voltage in the frequency band of over 5 GHz, and high conversion efficiency is also observed. By increasing the number of involved parallel stages, efficiency at higher input power levels is high (diode operation in the breakdown area at high power is dominant in decreasing the efficiency). The maximum achieved efficiency at the +20 dBm input power level is 67% when a single rectenna is used. The test-bench has been configured for a 12 V input and 5 V output at 1 A load.

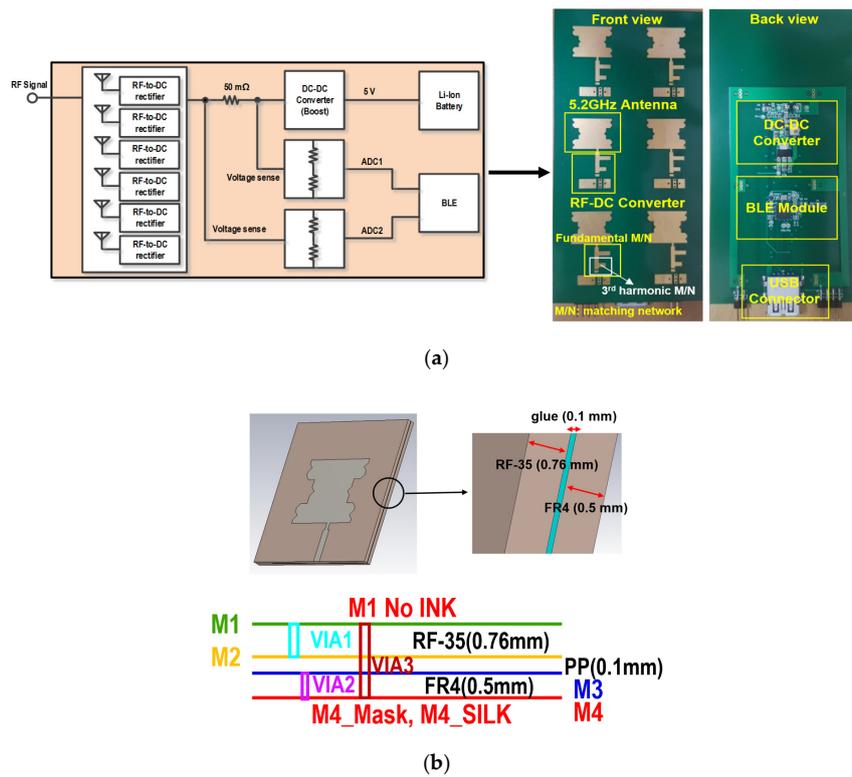


Figure 9. (a) Module of the fabricated RF RH, front (6-parallel rectenna) and back (Rx receiver) sides and (b) Information of the PCB layer (4 layers). Reprint with permission [4775431338148]; 2020, IEEE.

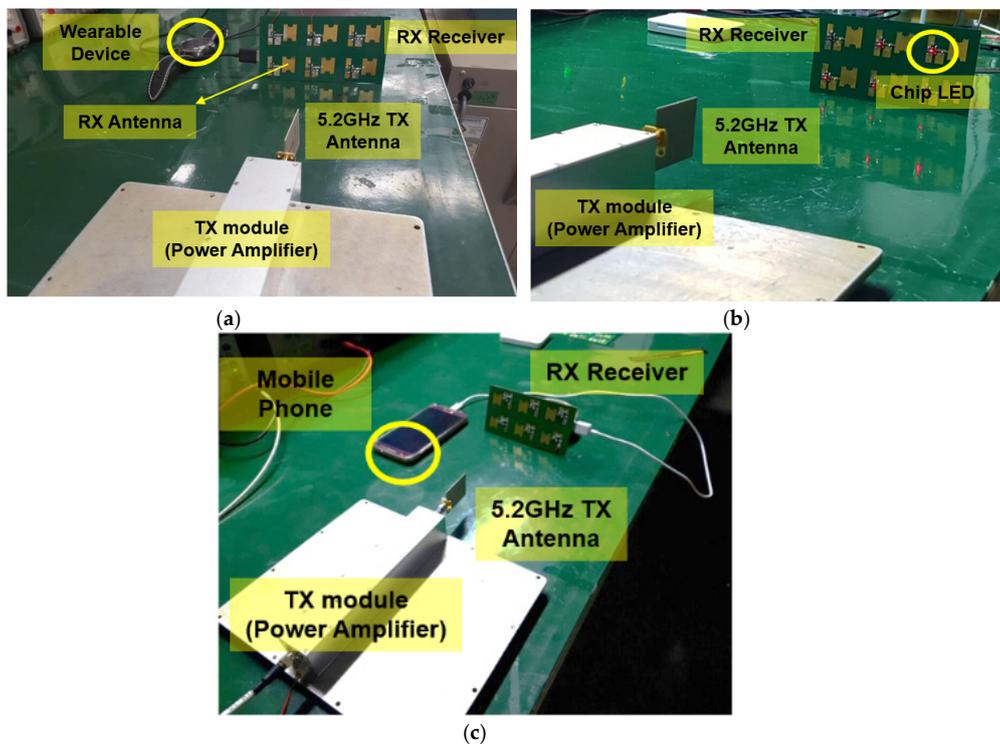


Figure 10. Test environment of the proposed RF EH (a) The Rx receiver board is connected to a G watch, (b) Chip LED, and (c) Mobile phone. Reprint with permission [4775431338148]; 2020, IEEE.

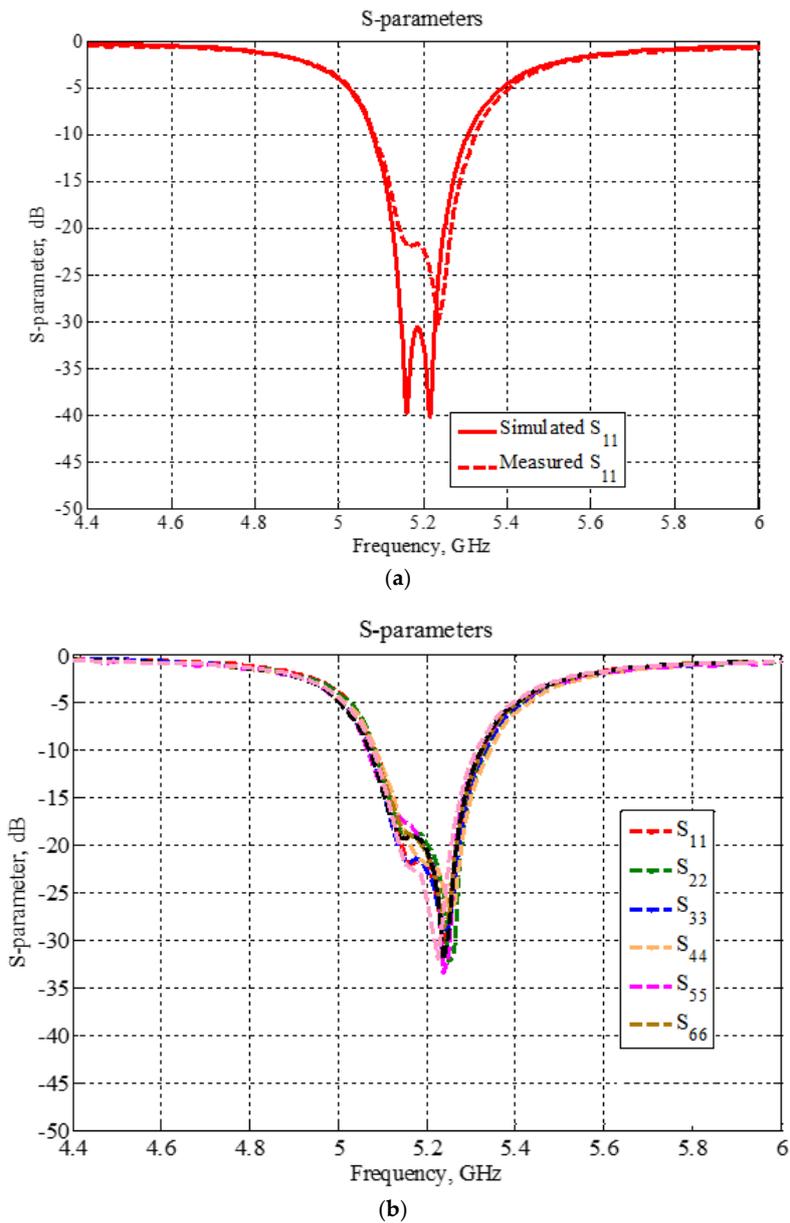


Figure 11. Reflection coefficient of (a) the Tx antenna and (b) 2 × 3 Rx antenna.

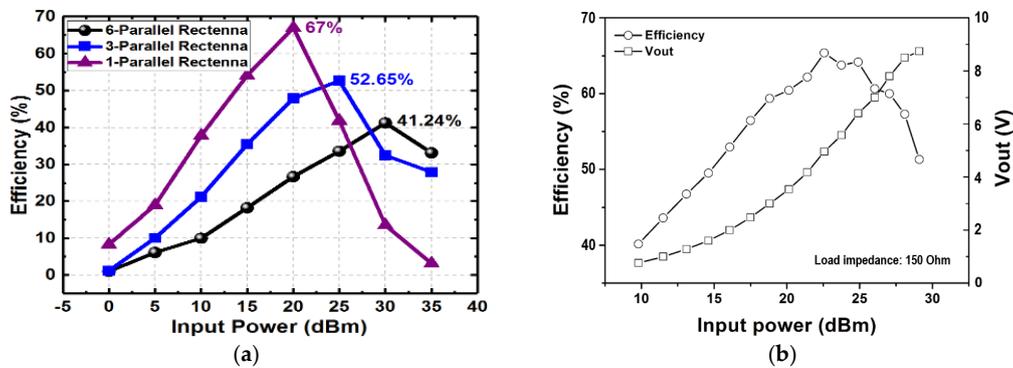


Figure 12. Measured efficiency vs. input power level of the proposed RF EH system (a) Different number of parallel rectenna stages and (b) Output voltages. Reprint with permission [4775431338148]; 2020, IEEE.

The simulation result of the buck-boost converter is illustrated in Figure 13. The maximum efficiency of the buck-boost converter reaches 93% at 2 MHz switching frequency. The measured functional performance of the RF EH harvester system is illustrated in Figure 14. Table 2 lists the important metrics of the RF RH system including key features, elements used in the Rx module, and PCB boards. Table 3 summarizes the whole performance of the RF EH. During the measurement, the USB connector is connected to IoT/wearable devices such as a G watch, LED, and cell phone.

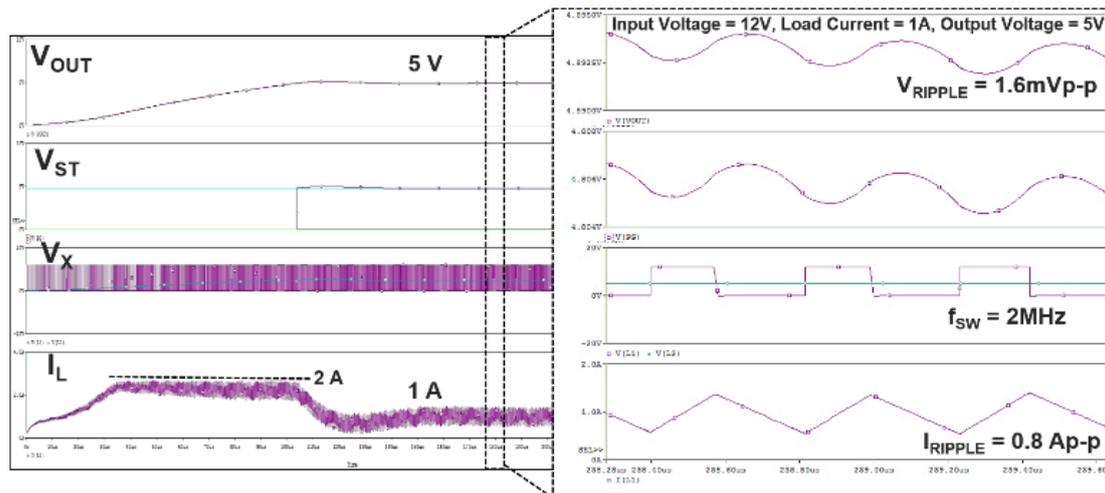


Figure 13. Simulation results of the buck-boost DC-DC converter. Reprint with permission [4775431338148]; 2020, IEEE.

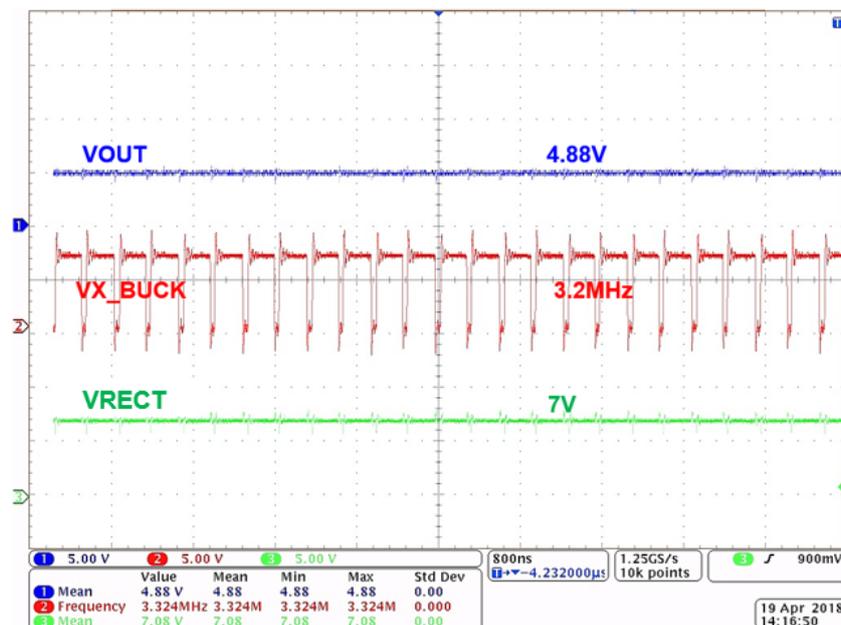


Figure 14. Measured results of the RF EH harvester.

Table 2. Performance Summary. Reprint with permission [4775431338148]; 2020, IEEE.

Parameter	Test Board
RF-DC converter type	6-parallel rectenna
Key features	1. Diode reliability considered 2. Parallel rectenna structure 3. Reconfigurable structure 4. Implementation for large input power
Diode	AVAGO HSMS-2862
Buck-boost converter	TI TPS63060
PCB board type	Taconic RF35 (Front: EH system) + FR4 (Back: BLE, DC-DC converter)
Peak efficiency	67% @20 dBm, 5.2 GHz

Table 3. Performance Summary of IoT/wearable Devices. Reprint with permission [4775431338148]; 2020, IEEE.

Parameter	LG G Watch (Wearable Device)	Mi Band (Wearable Device)	LG SmartThinQ (IoT, Sensor)
Battery capacity	400 mAh, 1.52 Wh	45 mAh, 0.17 Wh	300 mAh, 1.11 Wh
Battery Life ^a	24 h	30 day	90 day
Power Consumption	63 mW	0.24 mW	0.51 mW
Distance	25 cm	25 cm	25 cm
Transmission Power	30 dBm	30 dBm	30 dBm
Antenna Gain	20 dBi	20 dBi	20 dBi
Free Space Path Loss	−33.69 dB	−33.69 dB	−33.69 dB
Received Power	16.31 dBm	16.31 dBm	16.31 dBm
Battery charging time ^b	use time increased by 158%	8 h	36 h
Duration and use time aspects	use time increased by 158%	Continuous use without battery reduction when Tx Power is supplied	Continuous use without battery reduction when Tx Power is supplied

^a Battery Life = (Battery capacity [Wh]/Power Consumption [W]). ^b Battery charging time = (Battery capacity [mAh]/Charger output current [mA]) × Charging factor (1.2).

4. Conclusions

In this paper, an RF energy harvester based on a reconfigurable and multiple parallel rectenna with third harmonic control at the frequency band of 5.2 GHz was presented. In the proposed scheme, RF-DC conversion using a 6-parallel rectenna is realized. This approach provided high efficiency and output DC voltage level, which allowed the use of a simple buck DC-DC converter after the RF-DC converter. Finally, the buck DC-DC converter fixed the output voltage and supplied the IoT device or BLE chip. The presented architecture achieved maximum 67% power conversion efficiency and 6.1 V DC voltage at the input power level of +20 dBm. Using the proposed architecture, higher and different values of DC output voltage and power conversion efficiency can be obtained. Therefore, it can be used to power-up various IoT/wearable devices.

Author Contributions: H.A. designed and performed experiments, analyzed the data, and wrote the manuscript. A.H., B.S.R., S.Y.K., J.B., J.M.L., J.H.M., J.J.P., and Y.G.P. conceived and planned the simulation and measurements. A.H., B.S.R., S.Y.K., and Y.G.P. contributed to the design and implementation of the research, to the analysis of the results, and to the writing of the manuscript. K.C.H., Y.Y., D.I.K., and K.-Y.L. devised the project, the main conceptual ideas, and proof outline. K.-Y.L. supervised the project. All authors have read and agreed to the published version of the manuscript.

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