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Photovoltaic-Driven SiC MOSFET Circuit Breaker with Latching and Current Limiting Capability

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Abstract: This paper introduces a Solid State Circuit Breaker with Latching and Current Limiting capabilities for DC distribution systems. The proposed circuit uses very few electronic parts and it is fully analog. A SiC N-MOSFET driven by a photovoltaic driver and a maximum current detector circuit are the core elements of the system. This work details circuit operation under different conditions and includes experimental validation at 1 kVdc. Wide versatility, highly configurable, and very fast response, less than 1 µs in the case of short-circuit, are the most remarkable outcomes.

Keywords: Solid State Circuit Breaker (SSCB); fault current limiter; DC power distribution; WBG semiconductors; SiC MOSFET

1. Introduction

The ever-increasing number of DC loads in the domestic, public, and industrial sectors, together with the need to use renewable energies efficiently, is leading to the emergence of DC microgrids and end user distribution systems at higher voltages [1–6]. One of the key aspects, and one of the most challenging issues in DC microgrids and distribution relates to the protection system design [7]. The differences with AC distribution systems, such as arcing at disconnection [8], large capacitive loads that require high inrush currents and also produce very fast and large discharge electrical currents during low impedance faults [9], limit the use of traditional AC protection methods [10]. Commercial protection devices for DC distribution are typically fuses, Molded Case Circuit Breakers (MCCBs) and Solid State Circuit Breakers (SSCBs), the last group being those that use power semiconductor devices to decrease the tripping time and to increase the current interruption capability [11,12]. Silicon Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) devices, with low switching times and low on-resistance, are only adequate in low voltage DC distribution systems [13], i.e., below few hundreds of volts, while appropriate high-voltage, high-current power semiconductors, e.g., thyristors, Insulated-Gate Bipolar Transistor (IGBT), Integrated Gate-Commutated Thyristor (IGCT), are required in larger systems [14]. However, Wide BandGap (WBG) FET power transistors, with enhanced maximum voltage blocking capabilities, short switching times, and low on-resistance, have found new opportunities for SSCB development at higher voltages where silicon counterparts were not suitable [15].

In [16], the authors describe and experimentally validate a Silicon Carbide (SiC) Junction Field-Effect Transistor (JFET) based circuit breaker. This circuit, that uses a normally-on device, lacks current limitation capabilities and it could require additional protection methods to limit input surge currents. The gate drive circuit uses a small isolated PWM DC/DC converter that it is activated when a large fault current is detected by sensing the voltage across the JFET. Another related activity has been reported in [17], it deals with a circuit breaker based on SiC Static Induction Transistors (SIT) that uses an advanced control method for the gate voltage to reduce the voltage overshot during turn-off. It requires a digital processor, a high-speed digital-to-analog converter, an auxiliary supply,

and a current sensor. The concept has been evaluated with a 400 V and 12 A prototype for data center applications, proving to be effective reducing overvoltage and transient oscillation during the interruption process.

Gate drive circuits for SSCBs are also an important topic since their requirements are different to ones needed in other typical power electronic applications. In particular, in [18] the authors describe a gate driver circuit for series connected SiC MOSFETs used as solid state circuit breakers. In this context, a renewed interest in photonic power electronic devices has appeared [19]. In [20], the authors describe a bidirectional normally-on 1200 V SiC JFET circuit breaker that uses an optical signal to command the gate driver to turn off the power transistors; and more recently, in [21], an optically-isolated gate drive for SiC MOSFETs is investigated and compared with magnetically-coupled gate drivers.

Optically isolated photovoltaic drivers provide some advantages over other isolated driver circuits for SSCBs. Circuit breakers require isolation of DC signal, due to the long on or off periods. Unlike capacitive or transformer isolating circuits that require more complex signal refreshing circuits for DC signal isolation, photovoltaic circuits are well suited for this particular issue. They also have the capability to generate a variable analog signal which is required to operate the MOSFET in the linear region for current limiting applications. An additional benefit, that often is a drawback in other MOSFET driving applications, is the low photocell current that enables slow turn-on and enhances inrush current control and circuit stability. On the other hand, fast turn-off is desired to protect the system after load failure or off command. Thus, additional turn-off circuits are often employed, which in some cases are integrated on the photovoltaic driver. Authors introduced in [22] a new concept of DC protection which has been extended in this work.

To end this introductory section, the paper is organized as follows. Section 2 introduces the photovoltaic-driven Solid State Circuit Breaker with Latching and Current Limiting capabilities (SSCB-LCL). Section 3 details the different SSCB-LCL circuit configurations. Section 4 presents the setup and a main transistor robustness study. Section 5 illustrates the prototype design and explains the proposed test plan. Section 6 covers the experimental results and the subsequent discussion. The paper concludes with Section 6.

2. SSCB-LCL Description and Operating Principle

The proposed SSCB-LCL, represented in Figure 1, was developed using only discrete parts and in a simplified way operates as follows. If I_{Load} is lower than I_{Limit}, the SSCB-LCL will work in nominal operation, as a closed switch with very low conduction losses. In case I_{Load} exceeds I_{Limit}, the SSCB-LCL will limit the load current to I_{Limit} during a preconfigured time. If the fault persists, after the preconfigured time has elapsed, the load will be disconnected from the input. External commands were also included for controlled load disconnection or restarting the SSCB-LCL.

M_1 is an N-channel SiC MOSFET that is driven by PV_1 and Q_2 as the main current regulating element for I_{LED}. R_8 sets the maximum I_{LED} and V_1 and R_2 provide isolated supply to PV_1.

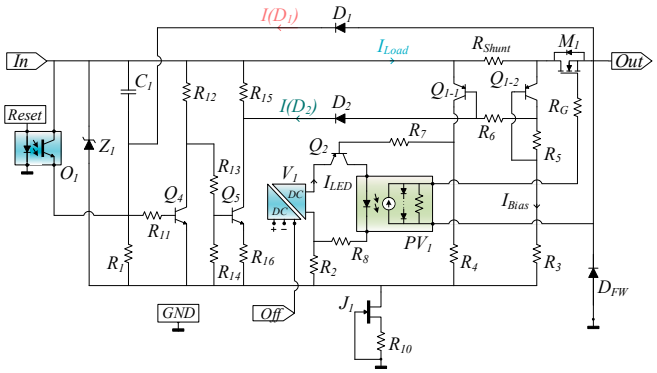

Figure 1. Electrical schematic of the proposed Solid State Circuit Breaker with Latching and Current Limiting capabilities (SSCB-LCL).

The current limiting loop comprises the dual matched NPN transistors, $Q_{1\text{-}1}$ and $Q_{1\text{-}2}$, R_{Shunt}, and biasing and gain resistors R_3, R_4, and R_5. During an overcurrent, this arrangement creates a current feedback loop that forces M_1 to operate in linear mode by changing V_{GS}. This circuit contains very few components, does not require external supply, and provides large bandwidth control signal for Q_2. In essence, $Q_{1\text{-}1}$ controls I_{LED} through Q_2 to close the current limiting feedback loop when the voltage across R_5 equals the voltage in R_{Shunt}. Under these circumstances, and assuming $V_{EB}(Q_{1\text{-}1}) = V_{EB}(Q_{1\text{-}2})$ and $I_B(Q_{1\text{-}1}) = I_B(Q_{1\text{-}2}) = 0$, the current is regulated to I_{Limit} (Equation (1)). Assuming $V(Z_1) >> (I_{Load}R_{Shunt} + V_{EB}(Q_{1\text{-}2}))$, I_{Bias} is given by Equation (2).

$$I_{Limit} = \frac{I_{Bias}R_5}{R_{Shunt}}, \tag{1}$$

$$I_{Bias} = \frac{V(Z_1)}{R_3}. \tag{2}$$

$t_{Latching}$ is defined as the time elapsed from the instant when I_{Load} exceeds I_{limit} until the moment when the latching circuit finally opens M_1. The timing function is performed with R_1 and C_1 depending on the status of D_1. Selecting $R_{11} >> R_1$, $V(Z_1) >> V(D_1)$ and assuming $V_{BE}(Q_4) + V(R_{11}) \cong 1V$, $t_{Latching}$ is approximated by Equation (3) and it can be easily adjusted by R_1 and C_1. The other parts, R_{11}, R_{12}, R_{13}, R_{14}, R_{15}, R_{16}, Q_4, Q_5, and D_2, form an accurate latching circuit to maintain M_1 in *Off-state* after $t_{Latching}$ has expired.

$$t_{Latching} = R_1C_1ln[V(Z_1)]. \tag{3}$$

Z_1 trims a proper voltage reference. The current source, J_1-R_{10}, was used to provide the bias current for Z_1 and the rest of SSCB-LCL. This current must be carefully adjusted to avoid excessive losses in J_1. For this reason, and due to the I_{LED} current requirements, V_1 is used for supplying I_{LED}. The enable input of V_1 provides the shutdown command (*Off*). In case of V_1 failure, the SSCB-LCL will be automatically disconnected. An opto-isolated *Reset* (O_1) input has been included for restarting the SSCB-LCL and a freewheeling diode (D_{FW}) is used to handle inductive load currents.

Focusing on MOSFET driver, the schematic diagram of PV_1 is shown in Figure 2a and the typical photocell current-to-voltage characteristics are shown in Figure 2b. Here, I_{LED} is controlled linearly by $I_B(Q_2)$ as given in Equation (4) (please refer to Figures 1 and 2b). $I_{LED_{max}}$ takes place when Q_2 is saturated (Equation (5)). Typically, I_{SC} is highly linear with I_{LED} (Equation (6)). The current-to-voltage dependence of a photocell can be represented by the single-diode cell model (Equation (7)) and the maximum voltage of PV_1 is then given by (Equation (8)).

$$I_{LED} = \beta I_B(Q_2), \tag{4}$$

$$I_{LED_{max}} = \frac{V_1 - V_{EC}\left(Q_{2_{Sat}}\right) - V_{LED}}{R_8}, \tag{5}$$

$$I_{SC} = \alpha I_{LED}, \tag{6}$$

$$I_{PhCell} = I_{SC} - I_R\left(e^{(V_{PhCell}\cdot\frac{q}{kT})} - 1\right), \tag{7}$$

$$V_{OC} = \frac{kT}{q}ln\frac{I_{SC}}{I_R}. \tag{8}$$

Detailed MOSFET *Turn-On* and *Turn-Off* processes can be explained with the help of Figure 3a,b (*Turn-On*) and Figure 3c,d (*Turn-Off*). MOSFET *Turn-On* using a photocell can be simplified as the C_{iss} charging with a constant current, I_{sc}. Two terms are clearly identified, $t_{d_{On}}$ and $t_{turn\text{-}On}$. $t_{d_{On}}$ depends on $Q_G(V_{th})$ (please refer to Figure 2c), and it is approximated by Equation (9). It could be adjusted with R_8 by modifying $I_{LED_{max}}$. On the other hand, $t_{turn\text{-}On}$, could be approximated by Equation (10) and

it can be also varied with R_8. The linear operation of M_1 can be achieved by keeping V_{GS} between the V_{th} and V_{OC}.

$$t_{d_{On}} \cong \frac{Q_G(V_{th})}{I_{SC}}, \tag{9}$$

$$t_{turn-On} \cong \frac{Q_G(V_{OC}) - Q_G(V_{th})}{I_{SC}}. \tag{10}$$

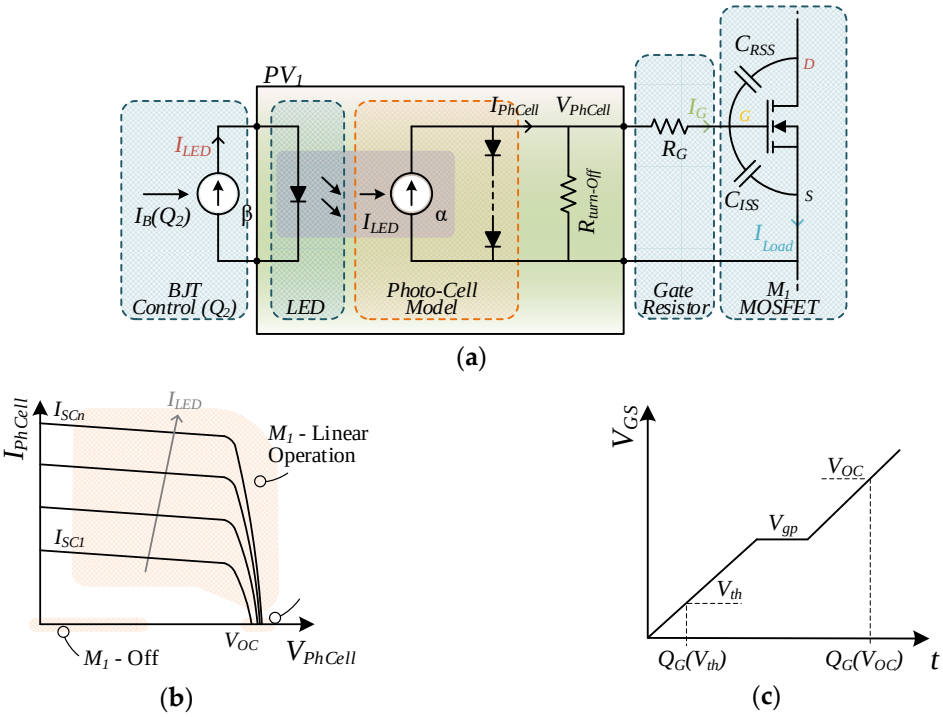

Figure 2. (**a**) Photovoltaic driving circuit block diagram. (**b**) Ideal current-to-voltage PV_1 characteristic. (**c**) Gate charge characteristic.

By contrast, MOSFET *Turn-off* can be seen as the C_{iss} discharging through the equivalent resistance $R_{turn-Off_{(Off)}}$. The process can be idealized using two time intervals, $t_{d_{Off}}$ and $t_{turn-Off}$. $t_{d_{Off}}$ is the time required to discharge C_{ISS} from V_{OC} to V_{gp}. It strongly depends on R_G and $R_{Turn-Off_{(Off)}}$ (please refer to Figure 3c,d), and it could be estimated by Equation (11). In addition, V_{gp} can be expressed in terms of V_{th}, g_{fs}, and I_{M_1} as in Equation (12).

$$t_{d_{Off}} = \left(R_G + R_{turn-Off_{(Off)}}\right) C_{ISS} ln \frac{V_{OC}}{V_{gp}}, \tag{11}$$

$$V_{gp} = V_{th} + \frac{I_{M_1}}{g_{fs}}. \tag{12}$$

Further, assuming inductive clamping behavior, $t_{turn-Off}$ can be split into two additional terms, t_{rv} and t_{fi}, which can be expressed as Equation (13) (please refer to Figure 3d).

$$t_{turn-Off} = t_{rv} + t_{fi} = \left(R_G + R_{turn-Off_{(Off)}}\right) \cdot \left(C_{RSS} \frac{V_{in}}{V_{gp}} + C_{ISS} ln \frac{V_{gp}}{V_{th}}\right). \tag{13}$$

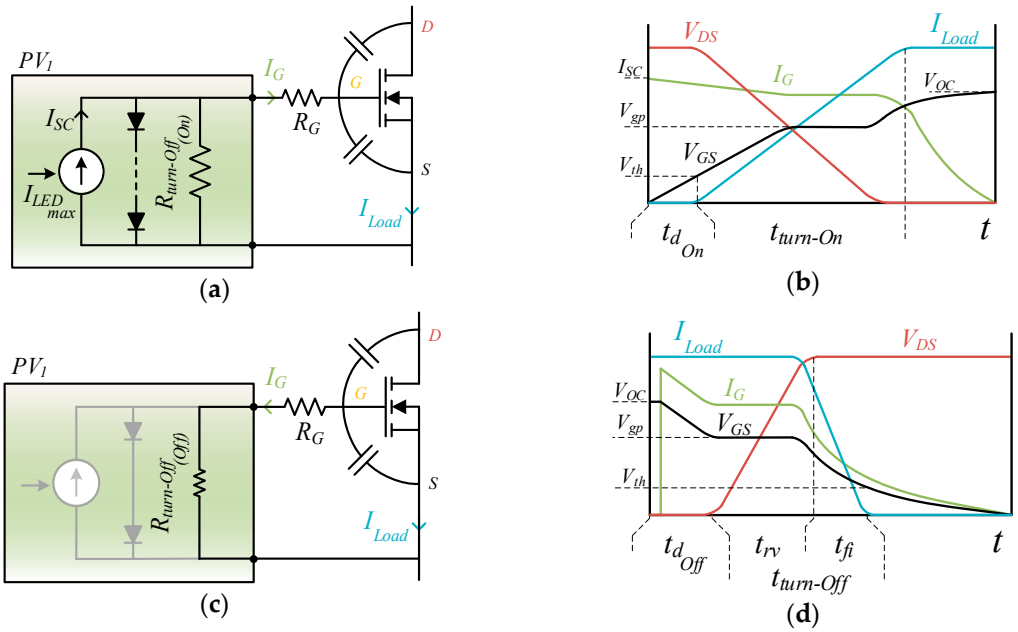

Figure 3. (**a**) Simplified Turn-On circuit; (**b**) Turn-On transient sketch; (**c**) simplified Turn-Off circuit; (**d**) Turn-Off transient sketch.

In response to an overcurrent fault, the SSCB-LCL operates in four different states, which are identified as *On-state*, *Delay State*, *Current Limiting State*, and *Off-State*. Please refer to Figure 4 for the equivalent schematic of each state.

During *On-State*, M_1 is fully on and I_{Load} shall remain below I_{Limit}. Under these conditions, $Q_{1\text{-}1}$ is off, Q_2, which is in saturation mode, provides I_{LEDmax} and $V_{GS} = V_{OC}$. Further, D_1 forces C_1 to keep discharged and Q_4 remains off. Please refer to Figure 4a.

Just after I_{Load} exceeds I_{Limit}, the SSCB-LCL enters in *Delay State*, I_{fault} flows through M_1 even though I_{LED} has been removed. The interval in *Delay State* is defined by $t_{d_{Off}}$. Further, D_1 turns off and C_1 starts charging. Please refer to Figure 4b.

After *Delay State* the SSCB-LCL automatically enters in *Current Limiting State*. In this state, $I_B(Q_2)$ is adjusted to keep I_{Limit} flowing through M_1 by operating it in linear region (Equation (1)). *Current Limiting State* automatically expires after $t_{Latching}$ (Equation (3)). At this point, $V(R_1)$ turns on Q_5 and D_2, then the SCCB-LCL latches in *Off-State* (refer to Figure 4d). *Current Limiting State* can be used, among other things, to limit inrush current with capacitive loads.

An external *Reset* is required to discharge C_1 to turn on the SSCB-LCL again. Please refer to Figure 1.

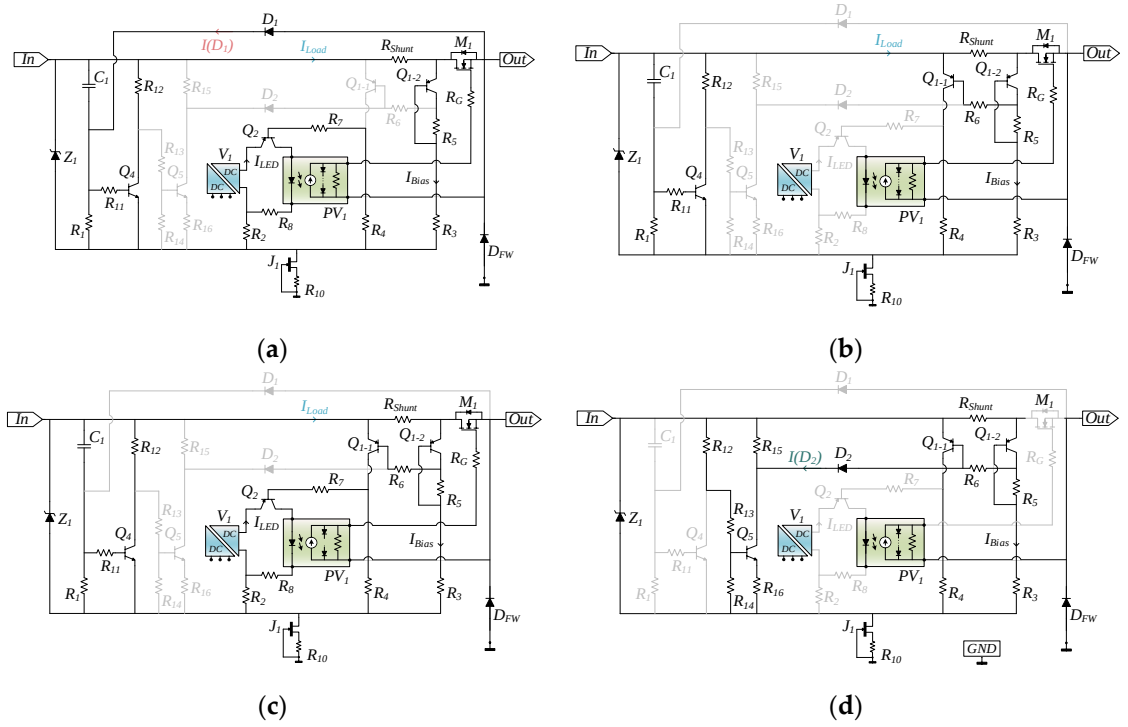

Figure 4. Equivalent circuits of each SSCB-LCL state; (**a**) *On-State*; (**b**) *Delay state*; (**c**) *Current Limiting State*; (**d**) *Off-State*.

3. SSCB-LCL Circuit Configuration

The SSCB-LCL allows different configurations by selecting R_G, R_1, and C_1. The three main configurations were named *STO with Current Limitation*; *FTO with Current Limitation*; *FTO without Current Limitation* (*circuit breaker*). The transient response is different for each configuration (please refer to Figure 5). These are described next:

3.1. STO with Current Limitation

This configuration is devised to provide smooth transition from *Delay State* to *Current Limiting State* (refer to Figure 5a). For this purpose, a large R_G value is used, typically above few kΩ. The larger R_G, the smoother the transition is to *Current Limiting State* and less overshot occurs; however, $t_{d_{Off_{STO}}}$ increases proportionally and its value must be carefully selected to avoid excessive delay. Under these conditions, $R_{Turn-Off_{(Off)}} << R_G$ applies and $t_{d_{Off_{STO}}}$ is eventually approximated by Equation (14).

$$t_{d_{Off_{STO}}} = R_G \cdot C_{ISS} \cdot ln \frac{V_{OC}}{V_{gp}}. \quad (14)$$

3.2. FTO with Current Limitation

This circuit configuration, which main waveforms are represented in Figure 5b, is intended to minimise $t_{d_{Off_{FTO}}}$ by eliminating R_G. In this case, $t_{d_{Off_{FTO}}}$ could be approximated by Equation (15). It is also worth indicating that M_1 turns off completely before entering in *Current Limiting State*, so, $t_{d_{On}}$ (Equation (9)) and $t_{Turn-On}$ (Equation (10)) apply after the current fault.

$$t_{d_{Off_{FTO}}} = R_{Turn-Off_{(Off)}} \cdot C_{ISS} \cdot ln \frac{V_{OC}}{V_{gp}}. \quad (15)$$

In both configurations, *STO with current limitation and FTO with current limitation*, $t_{d_{lmt}}$, and t_{lmt} can be approximated in terms of M_1 gate charge and I_{SC} as indicated by Equations (16) and (17), respectively.

$$t_{d_{lmt}} = \frac{Q_G(V_{OC})}{I_{SC}}, \tag{16}$$

$$t_{lmt} = R_1 C_1 ln[V(Z_1)] - \frac{Q_G(V_{OC})}{I_{SC}}. \tag{17}$$

3.3. FTO without Current Limitation (Circuit Breaker)

The SSCB-LCL can also be configured as a *circuit breaker* selecting the $t_{Latching}$ shorter than $t_{d_{On}}$. This feature, combined with *Fast Turn-Off*, is interesting to provide high-speed protection (please refer to Figure 5c for the main waveforms). This particular configuration must be adopted in applications where the appearance of a low inductance short-circuit is feasible.

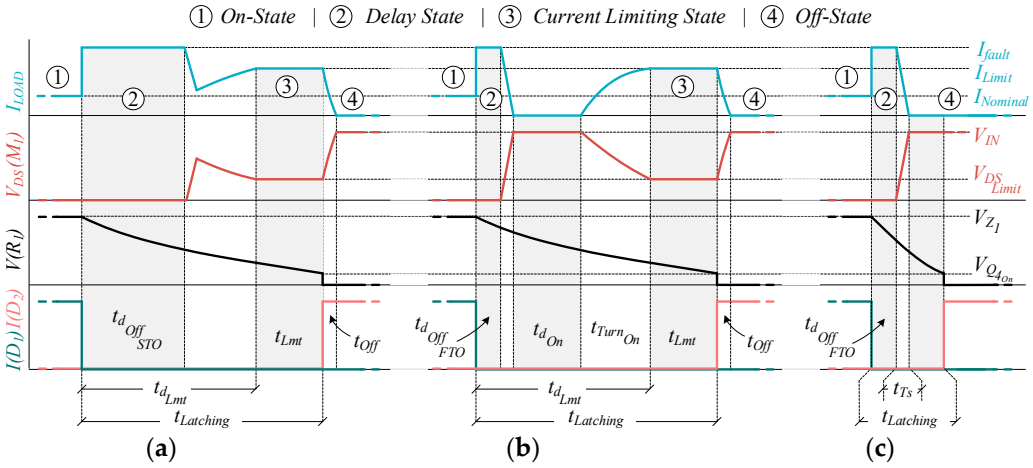

Figure 5. Idealized waveforms of each circuit configuration. (**a**) *STO with Current Limitation*; (**b**) *FTO with Current Limitation*; (**c**) *FTO without Current Limitation* (circuit breaker).

4. Materials and Methods

4.1. Setup and Main Transistor Robustness

Regarding the experimental setup, a Keysight N8937A power supply unit was used. A bank of six 590 uF capacitors (947D591K132DJRSN—Cornell Dubilier) is connected in parallel with the power supply. The load consists in a bank of 10 Multicomp MC14683 power resistors. It performs 1 kW nominal power capability at 1 kV with 1.95 mH parasitic series inductance, and an isolated FPGA controlled driver allows configurable resistor shunting to produce different step load (SL) conditions. The oscilloscope used is a 1 GHz analog bandwidth mixed domain oscilloscope (Tektronix MDO3104) with high-voltage differential probes (THDP0200 and THDP0100) and current probes (TCP0030A and TCP303). Please refer to Figure 6 for a simplified setup schematic.

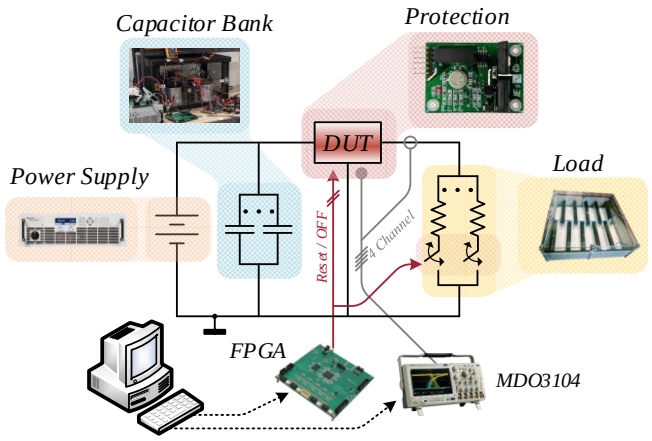

Figure 6. Sketch of the setup for the SSCB-LCL (DUT) validation.

The Wolfspeed C2M0080120D was chosen for M_1. Its robustness under high power dissipation conditions [23,24] makes it an excellent choice in the required power ratio.

Two critical conditions must be taken into account to guarantee M_1 robustness, operation in linear mode and short-circuit repetition capability.

For the first condition and to prevent M_1 damage by excessive energy dissipation, all time and current limits were set in compliance with the manufacturer's SOA, which means that selected limitation currents in the following tests are well below the specified current for switching applications shown in datasheets.

For the second condition, a C2M0080120D short circuit study was carried out. The study covers C2M0080120D ageing after 200 short-circuits at a V_{DS} = 1000 V with a V_{GS} = 8.4 V and a short-circuit time of 1.5 µs, longer than real response time in FTO *without Current Limitation* mode. Tests were realized at the Center of Reliable Power Electronics at the Aalborg University. Figure 7 shows the waveform evolution from the first and last (200) short circuit performed in these tests.

The data concludes that C2M0080120D is capable of withstanding at least 200 short-circuits at V_{DS} = 1000 V without appreciable degradation, resulting a longer useful life than the mechanical devices. In addition, the V_{GS} = 8.4 V condition means a reduction in the peak short-circuit current and shorter transition times according to Equations (11), (14) and (15). This condition furthermore allows low on-losses in low power range. D_{FW} partly alleviates the overvoltage when inductive loads are switched off. In [25] a new "soft turn-off" technique is proposed in order to reduce the voltage overshoot and short circuit peak current. In this work, the use of Digital Signal Processor to control the operation of the SSCB also allows other enhanced protection functions. A more detailed analysis of the robustness of C2M0080120D at 1000 V is presented in [26] where based on the aging parameters ($V_{GS(TH)}$, I_{DSS}, and R_{on}) analysis concluded that the C2M0080120D is capable to support, at least, 200 short circuits at 1000 V with 1.5 µs duration.

4.2. SSCB-LCL Design and Test Plan

An experimental prototype of the proposed SSCB-LCL was designed and implemented (please refer to Figure 8). Main part references are the following: M_1 is Wolfspeed C2M0080120D; Vishay VOM1271 as PV_1; 1N758 as Z_1; USCi UJN1205K as J_1, Traco Power TMR1-1211 as V_1 was used because it provides an on/off control input; Analog Devices MAT03 as $Q_{1\text{-}1}$ and $Q_{1\text{-}2}$; and Bourns PWR4412-2SCR0500F as R_{Shunt}.

Z_1 was biased with 1 mA while the whole biasing current flowing through J_1-R_{10} was 1.2 mA, so at 1 kV input voltage, J_1 dissipates around 1.2 W. On the other hand, I_{Bias} was adjusted to 145 µA. The values of R_5, R_1, C_1, and R_G were chosen depending on the performed test. Table 1 gathers all the relevant information of those values in each particular test.

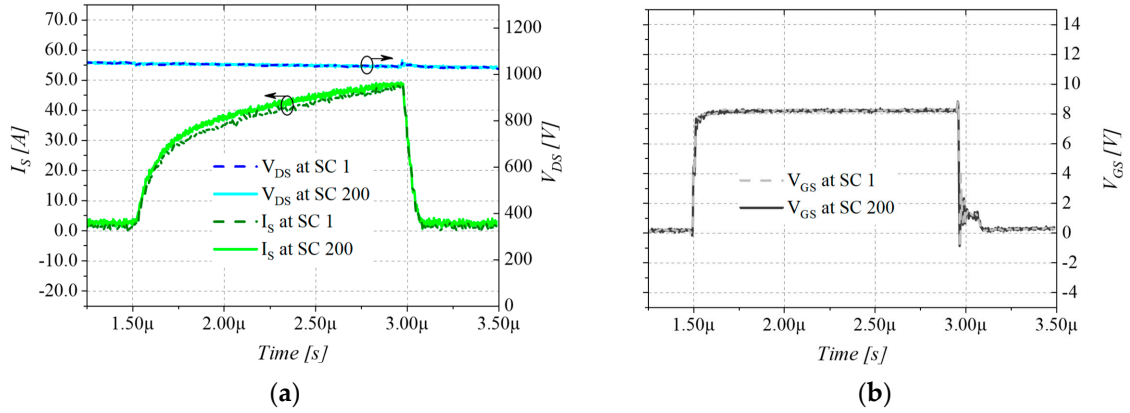

Figure 7. Short-circuit C2M0080120D test waveforms. (**a**) In dark blue dashed line V_{DS} in short circuit 1 (200 V/div); in cyan blue solid line V_{DS} in short circuit 200 (200 V/div); in dark green dashed line I_S in the short circuit 1 (10 A/div); in light green solid line I_S in the short circuit 200 (10 A/div). Time Scale: 0.5 µs/div. (**b**) In light grey dashed line V_{GS} in the short circuit 1 (10 A/div); In dark grey solid line V_{GS} in the short circuit 200 (2 V/div). Time scale: 0.5 µs/div.

The power loss of the device at nominal current, 1 A, is dominated by three factors. First, MOSFET conduction losses that are less than 0.1 W. The C2M0080120D equivalent on resistance, in conditions of V_{GS} = 8.5 V and a current of 1 A, is below 100 mΩ according to the manufacturer's data. Second, the current sink J_1-R_{10} dissipates around 1.2 W. Finally, the ancillary power supply specified 0.23 W of typical power losses. This eventually results in 1.5 W estimated power losses of the whole circuit.

Taking into account these considerations, the test plan was divided into three main groups: *STO with Current Limitation* under different soft-overload faults and parameter sweeps (from Test I to Test V); *FTO with Current Limitation* under soft-overload fault (Test VI); *FTO without Current Limitation* (*circuit breaker*) under short-circuit fault (Test VII) and telecommand test under soft-overload fault (Test VIII). All tests were carried out at 1 kV and the complete test description can be found in Table 1.

Table 1. Test description.

	Description	Constant Parameters		Variable Parameter
STO with Current Limiter	Test I Basic Operation	SL = 1 to 1.66 A $t_{Latching}$ = 4.5 ms I_{Limit} = 1.5 A	Load = 1000 to 600 Ω R_1 = 180 kΩ, C_1 =10 nF R_5 = 527 Ω, R_{Shunt} = 50 mΩ R_G = 180 kΩ	
	Test II R_G Sweep	SL = 1 to 2 A $t_{Latching}$ = 4.5 ms I_{Limit} = 1.5 A	Load = 1000 to 500 Ω R_1 = 180 k, C_1 = 10 nF R_5 = 527 Ω, R_{Shunt} = 50 mΩ	R_G = [50, 100, 180] kΩ
	Test III Overload Sweep	$t_{Latching}$ = 4.5 ms I_{Limit} = 1.5 A	R_1 = 180 kΩ, C_1 = 10 nF R_5 = 527Ω, R_{Shunt} = 50 mΩ R_G = 180 kΩ	LS = 1 A to [1.6, 2, 2.5, 3.3] A Load = 1000 Ω to [600, 500, 400, 300] Ω
	Test IV $t_{Latching}$ Sweep	SL = 1 to 2 A I_{Limit} = 1.5 A	Load = 1000 to 500 Ω R_5 = 527 Ω, R_{Shunt} = 50 mΩ R_1 = 180 kΩ, R_G = 180 kΩ	$t_{Latching}$ = [1.9, 4.1, 9.1] ms C_1 = [4.7, 10, 22] nF
	Test V I_{Limit} Sweep	SL = 1 to 2 A $t_{Latching}$ = 4.5 ms	Load = 1000 to 500 Ω R_1 = 180 k, C_1 = 10 nF R_G = 180 kΩ, R_{Shunt} = 50 mΩ	I_{Limit} = [1.25, 1.53, 1.80] A R_5 = [430, 527, 620] Ω

Table 1. *Cont.*

Description		Constant Parameters		Variable Parameter
Test VI ***FTO with Current Limitation***		SL = 1 to 2 A $t_{Latching}$ = 4.5 ms I_{Limit} = 1.5 A	Load = 1000 to 500 Ω R_1 = 180 k, C_1 = 10 nF R_5 = 527 Ω, R_{Shunt} = 50 mΩ R_G = 0 Ω	
Circuit Breaker	Test VII Short-circuit	SL = 1 A to SC I_{Limit} = 1.5 A	Load = 1000 Ω to SC R_5 = 527 Ω, R_{Shunt} = 50 mΩ R_1 = 510 Ω, C_1 = 1 nF R_G = 0 Ω	
	Test VIII Tele Command	SL = 1 to 2 A I_{Limit} = 1.5 A	Load = 1000 to 500 Ω R_5 = 527 Ω, R_{Shunt} = 50 mΩ R_1 = 510 Ω, C_1 = 1 nF R_G = 0 Ω	

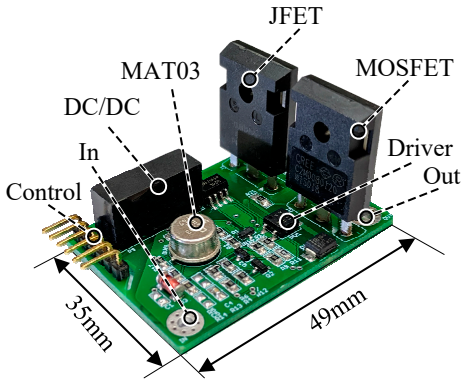

Figure 8. Implemented SSCB-LCL prototype.

5. Experimental Results and Discussion

To guarantee the long-term reliability, I_{Limit} and $t_{Latching}$ (from Test I to Test VI) were configured taking into account the Safe Operating Area (SOA) of M_1 plus some security margin (please refer to Figure 9).

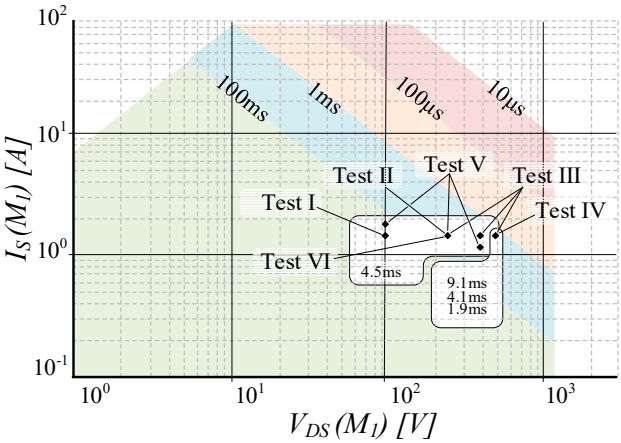

Figure 9. C2M0080120D datasheet Safe Operation Area and theoretical performed test location.

5.1. Basic Operation

The aim of this test was to corroborate the predicted circuit operation, especially the relation between I_{LED} and the SSCB-LCL response. As can be observed in Figure 10a, I_{LED} is I_{LEDmax} during

On-State and it is quickly removed when the fault is detected and it remains zero during $t_{d_{Off}}$. Then, it increases as the circuit enters into *Current Limiting State*, keeping M_1 in linear operation. Finally, I_{LED} goes to zero again when $t_{latching}$ elapses.

5.2. R_G Sweep

The objective was to observe the circuit response with different R_G values but keeping the same I_{limit}, $t_{latching}$, and step load. As can be observed in Figure 10b, $t_{d_{Off_{STO}}}$ increases with R_G but $t_{d_{lmt}}$ remains similar in all cases, as predicted by Equations (14) and (16). Since t_{lmt} is the same in all cases, M_1 experiences similar power stress during the current limiting state. Calculated and measured values for $t_{d_{Off_{STO}}}$ and $t_{d_{lmt}}$ are collected in Table 2. The following manufacturer's values were used for theoretical calculations: V_{OC} = 8.4 V; I_{SC} = 15 µA; C_{ISS} = 2 nF; V_{th} = 2.4 V; g_{fs} = 8 A/V. $Q_G(V_{OC})$ = 20 nC; $Q_G(V_{th})$ = 8.5 nC.

5.3. Overload Sweep

It was planned to observe the sensitivity of the SSCB-LCL to detect currents above I_{limit}, which were set to 1.5A. As can be seen in Figure 10c, only a small variation of $t_{d_{Off_{STO}}}$ is expected due to the change in V_{gp} (Equation (12)) produced by the different I_{fault}. Obviously, M_1 power dissipation increases as the load value in fault conditions decreases.

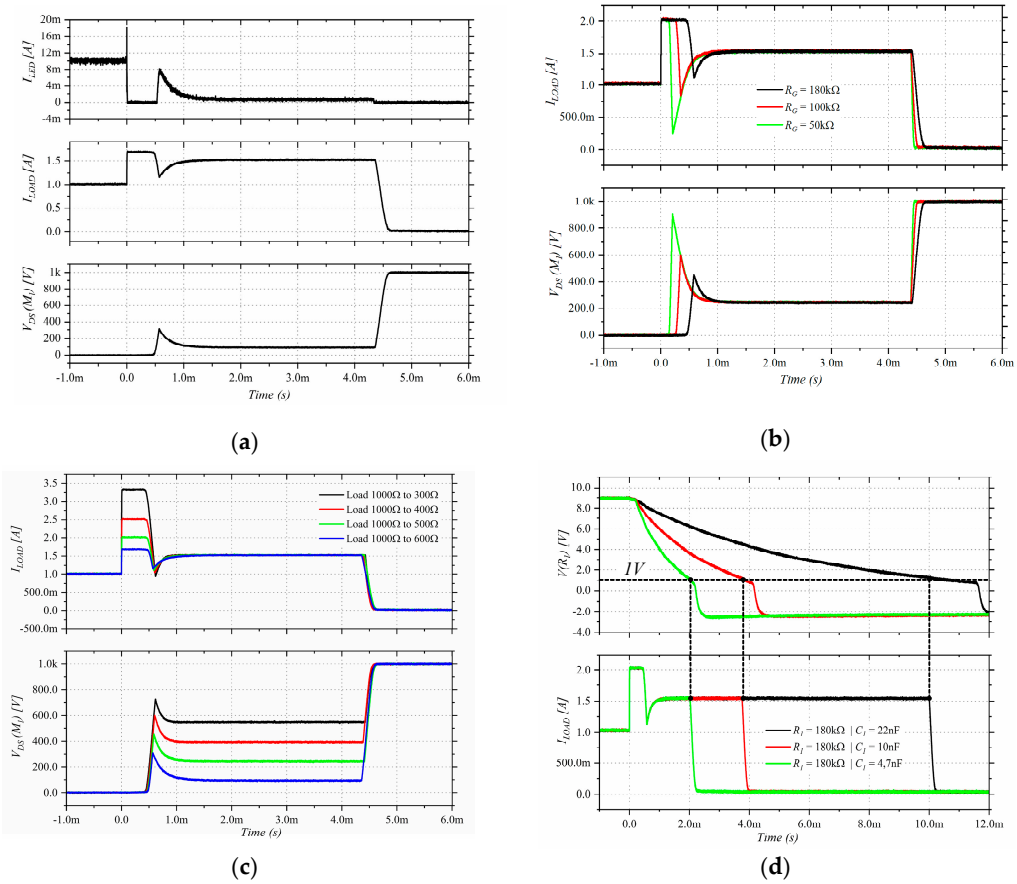

Figure 10. (**a**) *Test I—Basic Operation*. Top figure: I_{LED} (4 mA/div). Middle figure: I_{Load} (0.5 A/div). Lower figure $V_{DS}(M_1)$ (200 V/div). Time scale: 1 ms/div. (**b**) *Test II—R_G sweep*. Top figure: I_{Load} (500 mA/div). Lower figure: $V_{DS}(M_1)$ (200 V/div). Time scale: 1 ms/div. (**c**) *Test III—Overload sweep*. Top figure: I_{Load} (500 mA/div). Lower figure: $V_{DS}(M_1)$ (200 V/div). Time scale: 1 ms/div. (**d**) *Test IV—$t_{Latching}$ sweep* Top figure: $V(R_1)$ (1 V/div). Lower figure: I_{Load} (500 mA/div). Time scale: 1 ms/div.

5.4. $t_{Latching}$ Sweep

This test was performed to assess different $t_{Latching}$ in the *STO with Current Limitation* configuration. As reported in Table 2, calculated values (Equation (3)) are in good agreement with measured $t_{Latching}$. Figure 11d shows I_{Load} and R_1 voltage, which is a representative variable of the latching circuit.

5.5. I_{Limit} Sweep

In this test, several I_{Limit} (Equation (1)) were adjusted by modifying R_5 while keeping I_{Bias} = 145 µA. As can be observed in Table 2, good agreement is found between calculated and measured I_{Limit}, which also can be seen in Figure 11a.

5.6. FTO with Current Limitation

Test VI was carried out to evaluate the *FTO with Current Limitation* under soft-overload fault. For this test, R_G was set to 0 Ω. Table 2 and Figure 11b show the main results. It is worth to note the effect of M_1 source inductance, L_s, that creates a V_{DS} overvoltage during the turn-off.

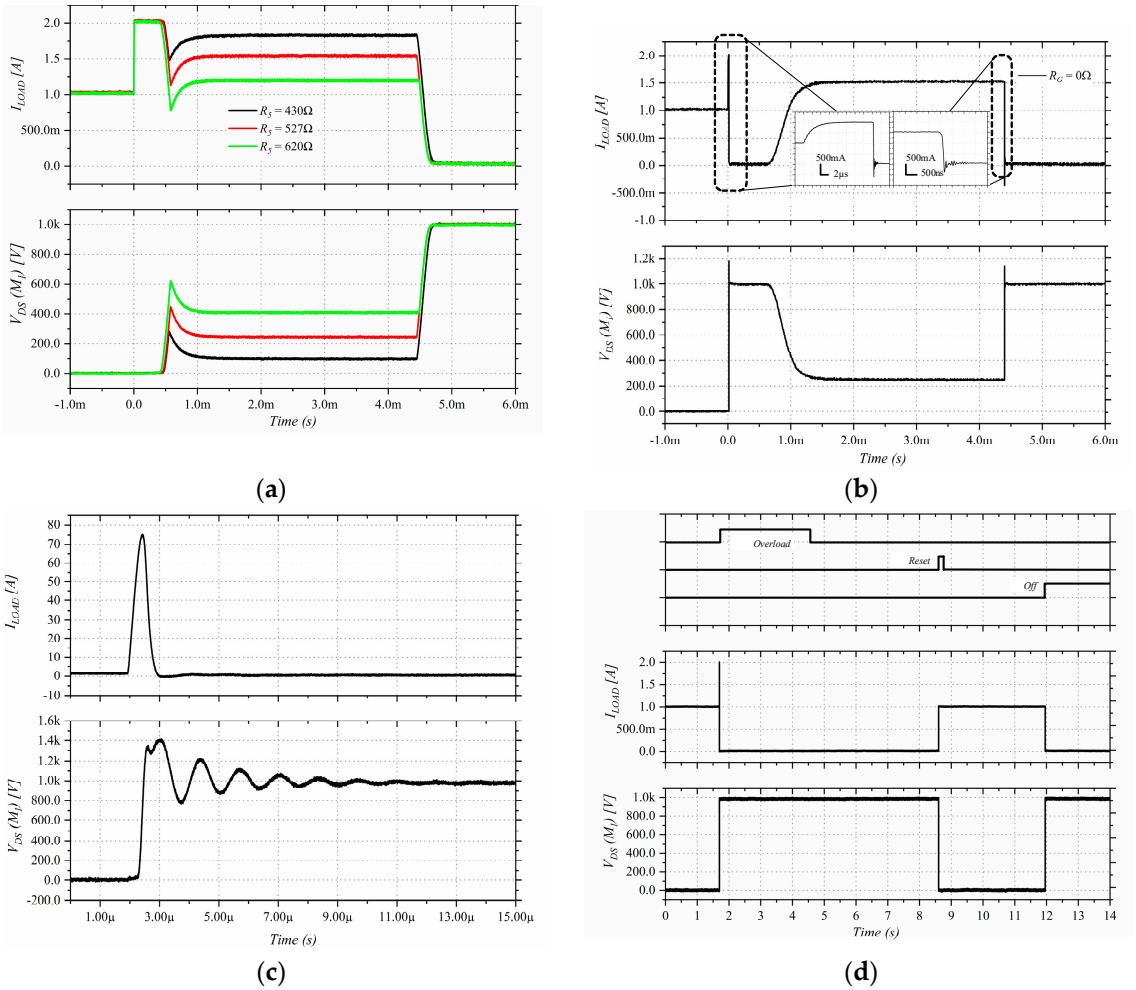

Figure 11. (**a**) *Test V—I_{Limit} sweep*. Top figure: I_{Load} (500 mA/div). Lower figure: $V_{DS}(M_1)$ (200 V/div). Time Scale: 1 ms/div. (**b**) *Test VI—FTO with current limitation.* Top figure: I_{Load} (500 mA/div). Lower figure: $V_{DS}(M_1)$ (200 V/division). Time scale: 1 ms/div. (**c**) *Test VII—Short circuit*. Top figure: I_{Load} (10 A/div). Lower figure: $V_{DS}(M_1)$ (200 V/div). Time scale: 1 µs/div. (**d**) *Test VIII—Tele Command Test.* Top figure: Digital *External Commands*. Middle figure: I_{Load} (500 mA/div). Lower figure: $V_{DS}(M_1)$ (200 V/div). Time scale: 1 s/div.

Table 2. Theoretical and test measured results.

	Description	Parameter	Variable		Theoretical	Measured
STO with Current Limiter	*Test II* R_G *Sweep*	$t_{d_{Off_{STO}}}$	R_G	50 kΩ	127 µs	146 µs
				100 kΩ	242 µs	264 µs
				180 kΩ	427 µs	462 µs
		$t_{d_{lmt}}$		*ALL*	1.3 ms	900 µs
	Test IV $t_{Latching}$ *Sweep*	$t_{Latching}$	C_1	4.7 nF	1.9 ms	2.2 ms
				10 nF	4.1 ms	4.0 ms
				22 nF	9.1 ms	10.2 ms
	Test V I_{Limit} *Sweep*	I_{Limit}	R_5	430 Ω	1.25 A	1.19 A
				527 Ω	1.53 A	1.54 A
				620 Ω	1.80 A	1.83 A
Test VI Fast Turn-Off with Current Limitation		$t_{d_{Off_{STO}}}$		*N/A*	N/A	16 µs
		$t_{d_{On}}$		*N/A*	570 µs	700 µs
		$t_{Turn-On}$		*N/A*	770 µs	700 µs

5.7. Short-Circuit

This test was proposed to evaluate the circuit response against a short-circuit event. In order to prevent linear operation of the MOSFET at such extreme conditions, FTO without Current Limitation configuration was chosen. As shown in Figure 11c, $t_{d_{Off_{FTO}}}$ is less than 1 µs, because V_{gp} (Equation (12)) goes closely to V_{OC} and gate discharge current tends to increase because of the source inductance effect.

5.8. Tele Command Test

Finally, Test VIII was performed to check the proper operation of *Tele-commands*. As represented in Figure 11d, a soft-overload (t = 1.7 s) produces the load disconnection. Then, fault condition extinguishes (t = 4.5 s) and the *Reset* command turns on (t = 8.6 s) the SSCB-LCL again. The *Off* signal (t = 12 s) finally switches off the SSCB-LCL.

6. Conclusions

This work deals with a Solid State Circuit Breaker with latching and current limiting capabilities. The most remarkable features of the circuit proposed are different configurations by changing simple component values, low power consumption, few discrete parts used, and easy parameter adjustment, i.e., current limit threshold and latching time. Theoretical assumptions and models were demonstrated with an experimental setup, and a large number of different tests were included, including the fast turn-off response under short-circuit events, less than 1 µs, and remote control at 1 kVdc. In order to explore the robustness of a particular device (i.e., C2M0080120D), the circuit test was performed close its maximum voltage limit, but voltage and current should be derated according to the final application. This circuit allows easy voltage and current scalability using an appropriate power MOSFET selection and gate driver design.

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Abbreviations

C_{ISS}	M_1 input capacitance.
C_{RSS}	M_1 reverse transfer capacitance.
g_{fs}	M_1 transconductance.
I_{Load}	Load current.
I_{Limit}	Programmed current limit.
I_{fault}	Fault current.
I_{Bias}	Bias current of current limiting circuit.
I_{LED}	PV_1 light emitting diode current.
$I_{LED_{max}}$	Maximum PV_1 light emitting diode current.
I_{SC}	PV_1 photocell short-circuit current.
I_R	PV_1 photocell diode saturation current.
M_1	Main power transistor.
PV_1	Photovoltaic driver.
$Q_G(V_{th})$	M_1 gate charge at its threshold voltage.
$Q_G(V_{oc})$	M_1 gate charge at the open circuit voltage of the PV_1 photocell.
R_{Shunt}	Shunt resistor.
R_G	M_1 gate resistor.
$R_{Turn-Off_{(Off)}}$	Equivalent resistance of PV_1 turn-off circuit during off state.
$R_{Turn-Off_{(On)}}$	Equivalent resistance of PV_1 turn-off circuit during on state.
$t_{Latching}$	Latching time.
$t_{d_{On}}$	Turn-on delay.
$t_{d_{Off}}$	Turn-off delay.
$t_{d_{Off_{STO}}}$	Turn-off delay in STO configuration.
$t_{d_{Off_{FTO}}}$	Turn-off delay in FTO configuration.
$t_{d_{lmt}}$	Current limitation response time.
t_{lmt}	Limitation time.
$t_{turn-On}$	Turn-on time.
$t_{turn-Off}$	Turn-off time.
t_{rv}	Voltage rise time.
t_{fi}	Current fall time.
V_{GS}	M_1 gate-source voltage.
V_{gp}	M_1 gate-source plateau voltage.
$V(Z_1)$	Reference voltage.
V_{LED}	PV_1 light emitting diode forward voltage
V_1	Auxiliary power supply.
V_{OC}	PV_1 photocell open circuit voltage.
V_{th}	M_1 threshold voltage.
V_{in}	SSCB-LCL input voltage.
α	PV_1 light emitting diode current to photocell current.
β	Bipolar junction transistor current gain.
k	Boltzmann's constant.
q	Electron charge.
FTO	Fast Turn Off.
STO	Slow Turn Off.

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