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Study on Fault Current Characteristics and Current Limiting Method of Plug-In Devices in VSC-DC Distribution System

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Abstract: The DC (Direct Current) distribution system based on the voltage source converter (VSC-DC) has become a research hotspot due to its various advantages. There are many plug-in devices in the VSC-DC distribution system, which may be damaged by the fault current. Therefore, studying the fault current characteristics and current limiting method is one of the key methods to ensure the safe and stable operation of the VSC-DC distribution system. Based on theoretical analysis and simulation calculations, this paper studies the causes, influencing factors, and current limiting methods of the fault current when the pole-to-pole fault occurs at the line side of plug-in devices in a ±10 kV VSC-DC distribution system. Firstly, based on the system topology, the decisive fault condition of fault current and the design principle of current limiting reactor value are analyzed. Secondly, the theoretical calculation methods of fault current and current limiting reactor value which satisfies the breaking capacity of DC circuit breaker are proposed. Finally, the accuracy of theoretical calculation methods is verified by simulation in PSCAD/EMTDC (Power Systems Computer Aided Design/Electromagnetic Transients including DC). The research results could provide the theoretical calculation methods of the fault current and the current limiting reactor value of plug-in devices in the ±10 kV VSC-DC distribution system.

Keywords: current limiting reactor; DC circuit breaker; fault current characteristics; plug-in devices; VSC-DC distribution system

1. Introduction

The DC distribution system based on the voltage source converter is advantageous to realize the renewable energy grid connection and consumption, sensitive electronic loads, and electric vehicles connection, etc. It will become one of the key technologies of smart energy and smart city development trend in the future [1,2]. At present, many ±10 kV VSC-DC distribution projects have been taken into application, such as Guizhou, Hangzhou, Zhangbei, Zhuhai ±10 kV VSC-DC distribution projects in China [3].

At present, there are still many basic scientific problems and key technologies concerning the VSC-DC distribution system that remain to be studied in depth. When the pole-to-pole fault occurs in the system, the fault current will rise rapidly due to the large-scale parallel capacitors. The capacitors installed in the converters will discharge directly through the short circuit point, which has a negative effect on the safe and reliable operation of the equipment and distribution power grid system. Therefore, studying on the fault current characteristics and current limiting method are of great significance for the design of the equipment, the control and protection strategy of the distribution system, etc.

At present, devices to isolate the DC faults mainly include AC (Alternating Current) circuit breakers, sub-modules with DC fault clearing capability, and DC circuit breakers [4]. Among them, AC circuit breakers have a longer operation time, which will expose power electronic devices to a larger fault current for a longer time and will also increase the time for the system to recover its power supply. The modified sub-modules with DC fault clearing capabilities will increase the loss and investment in steady state operation and complicate the control of the system at the same time. However, the DC circuit breakers have the advantages of fast operation speed and high reliability of system power supply. Therefore, using DC circuit breakers for fault isolation is an ideal choice in the VSC-DC system at present, and it is the major developing tendency. A living example is the Nan'ao multi-terminal VSC-DC project, which has installed DC circuit breakers to achieve fault isolation [5–8].

However, DC circuit breakers have low breaking capacity, which means that it cannot break a high fault current [9–13]. Therefore, it is necessary to limit the fault current within the DC breakers' breaking capacity by corresponding current limiting measures. Common current limiting methods include the use of series-connected inductance current limiter [14–16] and resistance current limiter [17–20], such as series current limiting reactor and superconducting current limiter. The principle of current limiting methods is to reduce the fault current by increasing the fault circuit impedance. At present, the simple and economical current limiting reactor is mainly adopted to limit the fault current [14,21].

Studying the causes of fault current and its electromagnetic transient characteristics can provide the theoretical basis for the design of system protection strategy and current limiting reactor. The study on fault current characteristics for a system protection strategy is based on a determined current limiting reactor, which cannot provide reference for the current limiting reactor selection [22–25]. However, there are still two deficiencies in the researches on current limiting methods [26–30]:

(1) The study on current limiting methods mainly focuses on the aspect of a single VSC converter when the pole-to-pole fault occurs at the line side. However, the interaction and protection methods of main converters and plug-in devices, which are connected to the medium voltage DC line, are neglected when the fault occurs.
(2) The study on current limiting methods of VSC converter mainly focuses on the main converter. However, the voltage level at the load side of the plug-in device is low, and the process of fault discharge is different from the main converter.

The reference [15] simulated and analyzed the fault current under the pole-to-pole fault at the line side of plug-in devices and selected the value of current limiting reactor. However, it did not propose any methods to select the value of current limiting reactor when the multiple plug-in devices were connected to the system.

Therefore, it is necessary to study the fault current electromagnetic transient characteristics and the current limiting method for the safe and stable operation of the plug-in devices and the whole system. The study is also useful for the protection strategy of plug-in devices [29,30]. Firstly, this paper analyzes and proposes the design principle of current limiting reactor value based on a VSC-DC distribution system, as the design scheme of Shenzhen Baolong Industrial Park [31,32]. Secondly, the causes of fault current are analyzed, and the theoretical calculation methods of fault current of plug-in devices are deduced. Thirdly, combined with the breaking capacity of medium voltage DC circuit breaker, the calculation methods of current limiting reactor value are proposed. At last, the electromagnetic transient simulations are carried out to verify the theoretical calculation methods of the fault current value and the current limiting reactor value. The value of fault current and current limiting reactor can be obtained quickly by the theoretical calculation methods in this paper, which has certain guiding significance for the construction of subsequent practical projects.

2. System Topology and Design Principle of Current Limiting Reactor Value

2.1. DC Distribution System Topology

The topology structure of the ±10 kV VSC-DC distribution system is shown in Figure 1. The system adopts ±10 kV unipolar symmetrical wiring method, and the loads are connected to the ±10 kV DC line through corresponding plug-in devices.

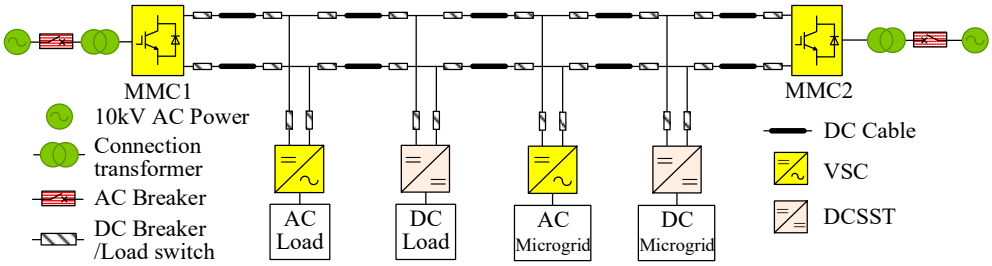

Figure 1. Topological structure of the ±10 kV VSC-DC distribution system.

System access loads include AC load, AC micro-grid, DC load, and DC micro-grid. Among them, the AC load and the AC micro-grid are connected to the ±10 kV DC cable through the two-level VSC converter. The DC load and the DC micro-grid are connected to the ±10 kV DC cable through the DC-DC transformer DCSST (DC Solid State Transformer) [31,32].

2.2. Design Principle of Current Limited Reactor Value

The typical pole-to-pole faults at the line side of plug-in devices of the VSC-DC distribution system are shown in Figure 2. In order to ensure that the DC circuit breaker can isolate the faults, the current limiting reactor should limit the fault current through the DC circuit breaker within its breaking capacity.

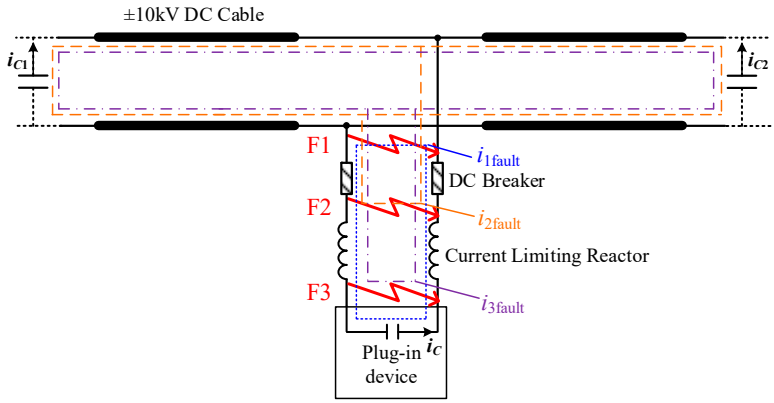

Figure 2. The possible pole-to-pole faults at the line side of plug-in devices.

When the F1 pole-to-pole fault occurs, the fault current through the DC circuit breaker i_{fault} is the discharge current i_C, which is the discharge current of the capacitor at the line side of plug-in device ($i_{1fault} = i_C$ in Figure 2). While in F2 or F3 pole-to-pole faults, the fault current through the DC circuit breaker i_{fault} is the sum of the discharge current from other devices' capacitors ($i_{2,3fault} = i_{C1} + i_{C2} + \ldots$ in Figure 2). Therefore, the more devices connect in the ±10 kV DC cable, the higher the fault current through the DC circuit breaker under F2 or F3 faults will be. Thus, the current limiting reactor value should be designed when all devices in the system are put into operation.

Compared with F3 fault, the fault current from other devices under F2 fault does not flow through the current limiting reactor of the plug-in device, so the fault current in F2 is more serious.

Therefore, only the F1 and F2 faults need to be considered when the limiting reactor value is designed, and the following two conditions should be satisfied:

(1) For F1 fault: the current limiting reactor should limit the discharge current from the capacitor at the line side of the plug-in device within the breaking capacity of the DC circuit breaker.
(2) For F2 fault: the sum of discharge current from the other device's capacitors should be limited to the breaking capacity of the DC circuit breaker.

3. Causes of Fault Current and Design Method of Current Limiting Reactor Value

3.1. F1 Pole-To-Pole Fault

3.1.1. Analysis of Pole-To-Pole Fault Current at the Line Side of VSC

When the plug-in device adopts VSC converter, AC load, and the low voltage AC micro-grid are connected to the ±10 kV DC cable through the VSC. For AC load, it will not discharge to the fault point after the fault, while for the AC micro-grid, compared with 10 kV, its voltage level is lower. At the same time, the discharge current is further reduced due to the impedance of transformer and the bridge arm inductor, so the discharge current can be neglected. Therefore, the fault development process can be divided into two stages when the F1 fault occurs at its line side.

The first stage, capacitor discharge stage: Because the discharge current of VSC load side is very low, and the current flowing through IGBT is similar with the normal operation, it will not cause IGBTs blocking. The blocking of IGBTs occurs when the DC circuit breaker operates. It is still necessary to consider the discharge of bridge arm reactor to the fault point. Therefore, the line side capacitor and the bridge arm inductor discharge through the fault point. The fault discharge circuit is shown in Figure 3. The fault discharge process can be superimposed by the second-order circuit of the capacitor–inductor and the first-order circuit of the inductor, as shown in Figure 4.

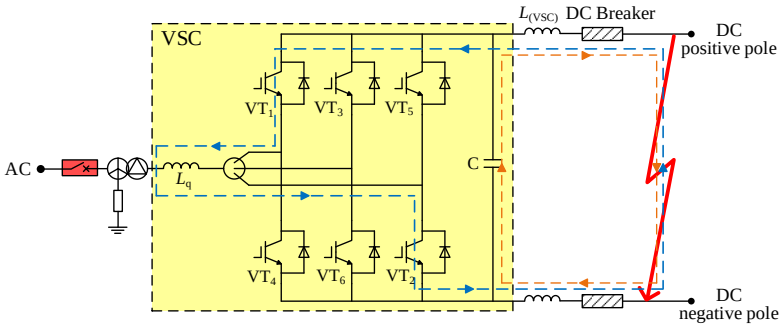

Figure 3. The first stage discharge circuit of VSC fault.

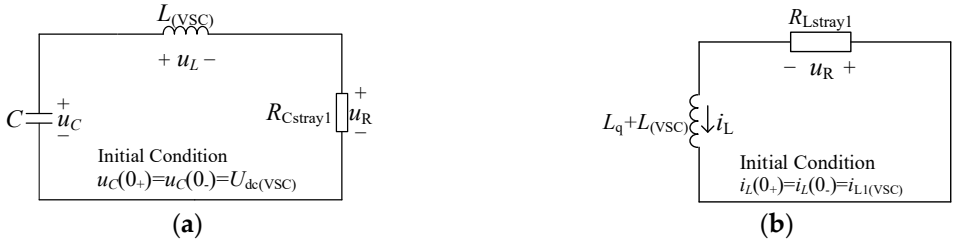

Figure 4. Equivalent circuit of the first stage discharge circuit of VSC: (**a**) capacitor and inductor discharge equivalent circuit and (**b**) inductor discharge equivalent circuit.

In Figure 4, R_{stray1} is the equivalent resistance of the first stage discharge circuit (where the capacitor discharge circuit equivalent resistance $R_{Cstray1(VSC)} = R_C + R_L + R_{DCB} + R_f$, bridge arm inductor discharge circuit equivalent resistance $R_{Lstray1(VSC)} = R_{Lq} + R_{IGBT} + R_L + R_{DCB} + R_f$), C is the

line side capacitor of VSC, $L_{(VSC)}$ is the current limiting reactor, L_q is the bridge arm reactor, U_{dc} is the voltage of capacitor, and $i_{L1(VSC)}$ is the line current.

The second stage, inductor freewheeling stage: when the voltage of the capacitor crosses zero, the reverse voltage applied to the diodes disappears and the diodes are turned on, as shown in Figure 5. When the energy stored in the current limiting reactor is exhausted, the fault discharge process ends. The equivalent circuit of the inductor freewheeling stage is shown in Figure 6.

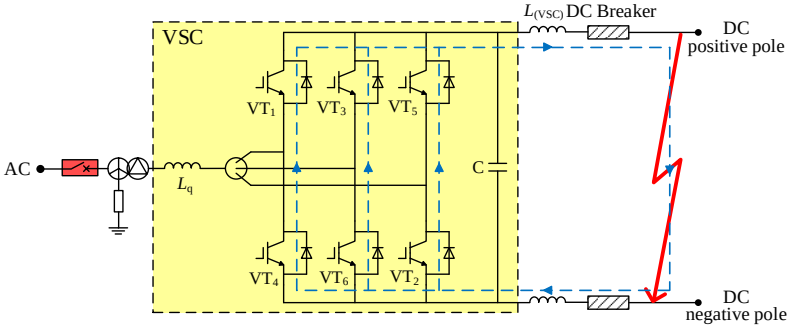

Figure 5. The second stage discharge circuit of VSC fault.

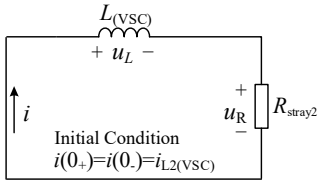

Figure 6. Equivalent circuit of the second stage discharge circuit of VSC.

In Figure 6, R_{stray2} is the equivalent resistance of the second stage discharge circuit ($R_{stray2(VSC)} = R_D + R_L + R_{DCB} + R_f$), $L_{(VSC)}$ is the current limiting reactor, and $i_{L2(VSC)}$ is the instantaneous fault current before the start of the second stage.

The fault current calculation methods in different stages can be obtained from the fault equivalent circuit:

The first stage, capacitor discharge stage: the fault current $i_{F1(VSC)}$ is given by

$$i_{F1(VSC)} = i_{C_{(VSC)}} - i_{L_{(VSC)}} = e^{-\delta t}\frac{U_{dc(VSC)}}{\omega L(VSC)}\sin(\omega t) - iL1(VSC)e^{-\frac{t}{(L_{(VSC)}+Lq)/R_{Lstray1(VSC)}}} \quad (1)$$

where $\delta = \frac{R_{Cstray1(VSC)}}{2L(VSC)}$, $\omega = \sqrt{\frac{1}{L(VSC)C(VSC)} - \left(\frac{R_{Cstray1(VSC)}}{2L(VSC)}\right)^2}$.

The second stage, inductor freewheeling stage: the fault current $i_{F1(VSC)}$ is given by

$$i_{F1(VSC)} = i_{L2(VSC)}e^{-\frac{t}{L_{(VSC)}/R_{stray2(VSC)}}} \quad (2)$$

where $i_{L2_{(VSC)}} = e^{-\delta t_C}\frac{U_{dc(VSC)}}{\omega L(VSC)}\sin(\omega t_C) - iL1(VSC)e^{-\frac{t_C}{(L_{(VSC)}+Lq)/R_{Lstray1(VSC)}}}$.

The time of capacitor voltage crossing zero is given by

$$t_C = [\pi - \arctan(\frac{\omega}{\delta})]/\omega \quad (3)$$

From the analysis above, it can be seen that the rising stage of fault current under F1 fault is the capacitor discharge stage, and the decaying stage is the inductor freewheeling stage. Therefore, to limit the magnitude and the rising rate of the fault current, the capacitor discharge stage should be limited. The breaking capacity of the DC circuit breaker has two influencing factors: the maximum

breaking current, I_{DCB}, and the maximum breaking time, t_{DCB}. The DC circuit breaker can break the maximum fault current I_{DCB} within the time t_{DCB} (including fault identification time and breaking time). The relationship between I_{DCB} (t_{DCB}), VSC line side capacitor, and current limiting reactor (C, $L_{(VSC)}$) can be obtained from (1), and the calculation results are shown in Figure 7.

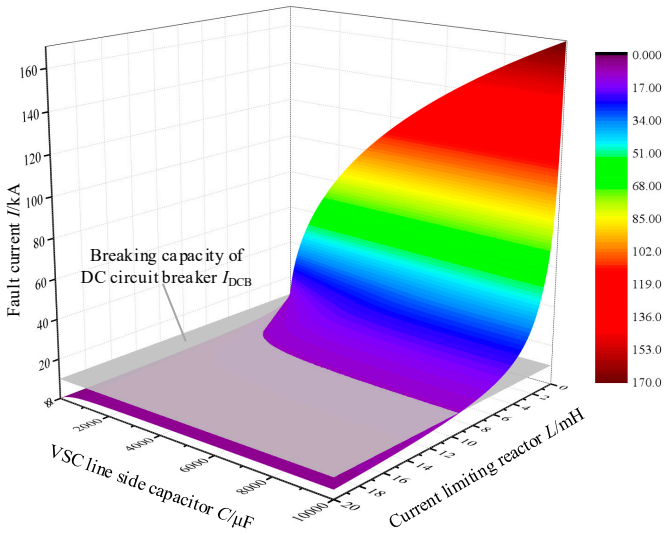

Figure 7. Effect of VSC line side capacitor and current limiting reactor (C, $L_{(VSC)}$) on the fault current of DC circuit breaker.

Figure 7 shows that the larger the capacitor or the smaller the current limiting reactor value is, the higher the fault current that flows through the DC circuit breaker will be. However, as the current limiting reactor increases, the effect of the capacitor on the fault current is reduced. Therefore, the value of current limiting reactor is the major factor affecting the fault current. It is more effective to limit the fault current by increasing the current limiting reactor value. In order to make the fault current satisfy breaking capacity of the DC circuit breaker (assuming I_{DCB} = 10 kA within t_{DCB} = 5 milliseconds), the parameters of the capacitor of VSC and current limiting reactor (C, $L_{(VSC)}$) should be in the blank area of Figure 8. It is found that when the breaking current I_{DCB} of DC circuit breaker goes higher, the current limiting reactor value can be lower.

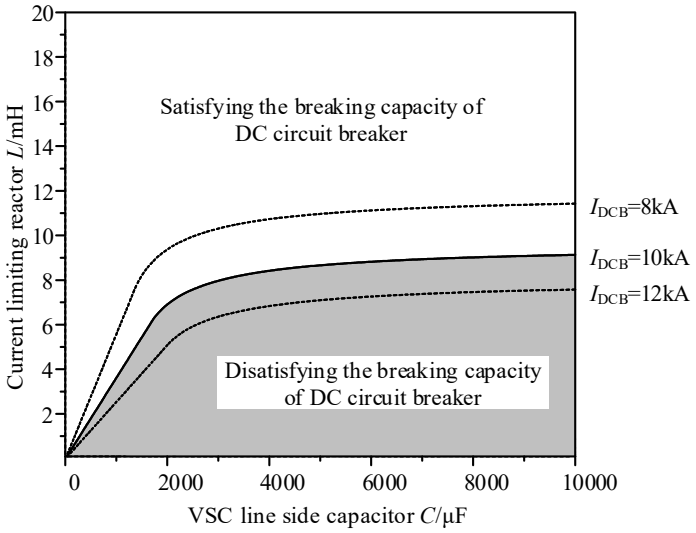

Figure 8. Relationship between DC circuit breaker breaking capacity I_{DCB} and VSC capacitor C, current limiting reactor $L_{(VSC)}$.

Therefore, when the F1 fault occurs at the line side of the VSC, in order to limit the fault current to the breaking capacity of the DC circuit breaker, the fault current $i_{F1(VSC)}$ should satisfy (4) in the capacitor discharge stage after the current limiting reactor $L_{F1(VSC)}$ is installed to the VSC.

$$i_{F1(VSC)} = e^{-\delta t}\frac{U_{dc_{(VSC)}}}{\omega L_{F1_{(VSC)}}}\sin(\omega t) - iL1(VSC)e^{-\frac{t}{(L_{F1(VSC)}+Lq)/R_{Lstray1(VSC)}}} \le I_{DCB}(t \le t_{DCB}) \quad (4)$$

where $\delta = \frac{R_{Cstray1(VSC)}}{2L_{F1}(VSC)}$, $\omega = \sqrt{\frac{1}{L_{F1}(VSC)C(VSC)} - \left(\frac{R_{Cstray1(VSC)}}{2L_{F1}(VSC)}\right)^2}$.

3.1.2. Analysis of Pole-To-Pole Fault Current at the Line Side of DCSST

When the plug-in device uses DCSST converter, the structure of which adopts high-frequency-link DC transformer topology (the equivalent topology structure is shown in reference [30]), the multiple modularization schemes are in the form of input series output parallel (ISOP) [33,34]. When F1 fault occurs at its line side, the fault development process is similar to VSC and can also be divided into two stages.

The first stage, capacitor discharge stage: compared with the VSC capacitor discharge process, there is no bridge arm inductor discharge process in DCSST, so that the fault discharge process is only equivalent to the second-order circuit of capacitor–inductor. The fault discharge circuit is shown in Figure 9. The fault discharge process can be superimposed by the second-order circuit of the capacitor–inductor, as shown in Figure 10.

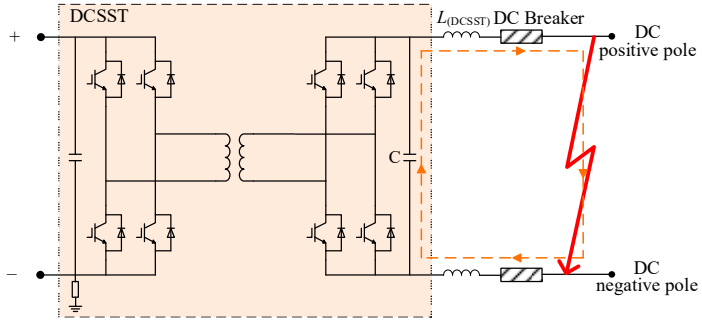

Figure 9. The first stage discharge circuit of DCSST fault.

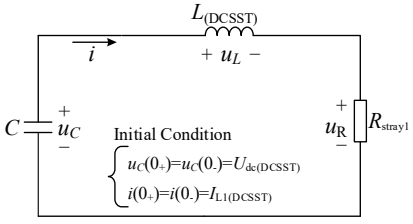

Figure 10. Equivalent circuit of the first stage discharge circuit of DCSST.

The second stage, inductor freewheeling stage: when the voltage of the capacitor crosses zero, the current limiting reactor will freewheel through the diode. The equivalent circuit is shown in Figure 7.

The fault current calculation methods in different stages can be obtained from the fault equivalent circuit:

The first stage, capacitor discharge stage: the fault current is given by

$$i_{F1(DCSST)} = e^{-\delta t}\left[\frac{U_{dc(DCSST)}}{\omega L(DCSST)}\sin(\omega t) - \frac{\omega_0 iL1(DCSST)}{\omega}\sin(\omega t - \beta)\right] \quad (5)$$

where $\delta = \frac{R_{\text{stray1(DCSST)}}}{2L(\text{DCSST})}$, $\omega = \sqrt{\frac{1}{L(\text{DCSST})C(\text{DCSST})} - (\frac{R_{\text{stray1(DCSST)}}}{2L(\text{DCSST})})^2}$, $\omega_0 = \sqrt{\frac{1}{L(\text{DCSST})C(\text{DCSST})}}$, $\beta = \arctan(\frac{\omega}{\delta})$.

The second stage, inductor freewheeling stage: the fault current is given by

$$i_{\text{F1(DCSST)}} = i_{\text{L2(DCSST)}} e^{-\frac{t}{L(\text{DCSST})/R_{\text{stray2(DCSST)}}}} \tag{6}$$

where $iL2(\text{DCSST}) = e^{-\delta t_C}[\frac{U_{\text{dc(DCSST)}}}{\omega L(\text{DCSST})}\sin(\omega t_C) - \frac{\omega_0 iL1(\text{DCSST})}{\omega}\sin(\omega t_C - \beta)]$.

The time of capacitor voltage crossing zero is given by

$$t_C = [\pi - \arctan(\frac{\omega}{\delta})]/\omega \tag{7}$$

The relationship among the DC breaker breaking capacity I_{DCB} (t_{DCB}), the DCSST capacitor, and the current limiting reactor (C, $L_{(\text{DCSST})}$) can be obtained from (4), which is similar to Figure 7. Similarly, a bigger DCSST current limiting reactor has a better current limiting effect, while the request for current limiting reactor value becomes lower when the breaking current I_{DCB} goes higher.

Therefore, when the F1 fault occurs at the line side of DCSST, the fault current should satisfy (8) in the capacitor discharge stage, and after that the current limiting reactor $L_{\text{F1(DCSST)}}$ is installed to the DCSST for the purpose of limiting the fault current to the breaking capacity of the DC circuit breaker.

$$i_{\text{F1(DCSST)}} = e^{-\delta t}[\frac{U_{\text{dc}_{(\text{DCSST})}}}{\omega L_{\text{F1(DCSST)}}}\sin(\omega t) - \frac{\omega_0 iL1_{(\text{DCSST})}}{\omega}\sin(\omega t - \beta)] \le I_{\text{DCB}}(t \le t_{\text{DCB}}) \tag{8}$$

where $\delta = \frac{R_{\text{stray1(DCSST)}}}{2L_{\text{F1}}(\text{DCSST})}$, $\omega = \sqrt{\frac{1}{L_{\text{F1}}(\text{DCSST})C(\text{DCSST})} - (\frac{R_{\text{stray1(DCSST)}}}{2L_{\text{F1}}(\text{DCSST})})^2}$, $\omega_0 = \sqrt{\frac{1}{L_{\text{F1}}(\text{DCSST})C(\text{DCSST})}}$, $\beta = \arctan(\frac{\omega}{\delta})$.

3.2. F2 Pole-To-Pole Fault

When the F2 fault occurs in the line side of the plug-in device, the fault current through the DC circuit breaker is the sum of discharge currents from the other devices, that is $i_{\text{fault}} = i_{\text{C1}} + i_{\text{C2}} + i_{\text{C3}} + i_{\text{C4}} + i_{\text{C5}}$, as shown in Figure 11. Therefore, in order to reach the breaking capacity of the DC circuit breaker, the fault current i_{fault} needs to satisfy $i_{\text{fault}} \le I_{\text{DCB}}$ ($t \le t_{\text{DCB}}$).

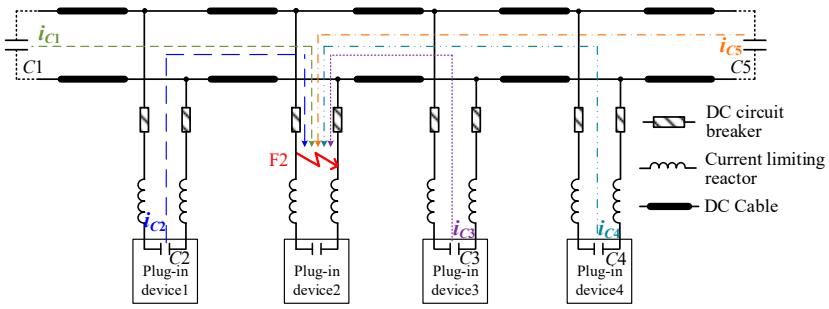

Figure 11. When F2 pole-to-pole fault occurs in plug-in device 2, other devices discharge to the fault point.

The capacitor discharge currents of VSC and DCSST under F2 fault are shown in (9) and (10).

$$i_{\text{F2(VSC)}} = \text{e}^{-\delta t}\frac{U_{\text{dc(VSC)}}}{\omega(L_{(\text{VSC})} + L_{\text{Cable}})}\sin(\omega t) - IL(\text{VSC})e^{-\frac{t}{(L_{(\text{VSC})}+L_{\text{Cable}}+Lq)/R_{\text{Lstray(VSC)}}}} \tag{9}$$

where $\omega = \sqrt{\frac{1}{(L_{(VSC)}+L_{Cable})C(VSC)} - \left(\frac{R_{Cstray(VSC)}}{2(L_{(VSC)}+L_{Cable})}\right)^2}$, $\delta = \frac{R_{Cstray(VSC)}}{2(L_{(VSC)}+L_{Cable})}$, $R_{Cstray(VSC)} = R_C + R_L + R_{Breaker} + R_{fault} + R_{Cable}$, $R_{Lstray(VSC)} = R_C + R_L + R_{Breaker} + R_{fault} + R_{Cable}$.

$$i_{F2(DCSST)} = e^{-\delta t}\left[\frac{U_{dc(DCSST)}}{\omega(L_{(DCSST)} + L_{Cable})}\sin(\omega t) - \frac{\omega_0 IL(DCSST)}{\omega}\sin(\omega t - \beta)\right] \quad (10)$$

where $\omega = \sqrt{\frac{1}{(L_{(DCSST)}+L_{Cable})C(DCSST)} - \left(\frac{R_{stray(DCSST)}}{2(L_{(DCSST)}+L_{Cable})}\right)^2}$, $\delta = \frac{R_{stray(DCSST)}}{2(L_{(DCSST)}+L_{Cable})}$, $\omega_0 = \sqrt{\frac{1}{(L_{(DCSST)}+L_{Cable})C(DCSST)}}$, $\beta = \arctan(\frac{\omega}{\delta})$, $R_{stray(DCSST)} = R_C + R_L + R_{Breaker} + R_{fault} + R_{Cable}$.

From the analysis above, it can be seen that the fault current through the DC circuit breaker is related to the line parameters, the number of devices, the capacitors of devices, and the value of current limiting reactors of each device. The fault current through the DC circuit breaker will be higher when the line is shorter, the number of plug-in devices is more, the current limiting reactors value are lower, and the capacitors of devices are larger.

In the initial stage of system design, in order to reduce the fault current, a longer line and a lesser number of the system devices should be considered if possible. Figure 12 gives an example of reducing the fault current as low as possible. It shows that the DC load and DC micro-grid are connected to the DC cable by the DC/DC transformer and the DC bus, while the AC voltage (including the AC Load and AC micro-grid) was converted to DC by the VSC converter.

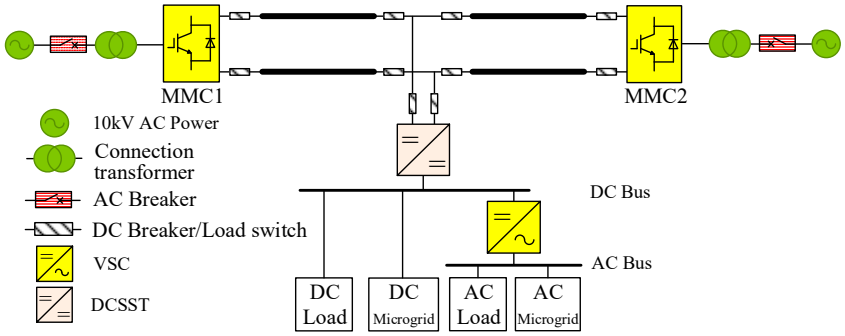

Figure 12. Topological structure of VSC-DC distribution system.

In order to ensure that the fault current of the DC circuit breaker is under its breaking capacity in F2 fault, the fault current generated by each device should be limited to $\frac{1}{N-1}I_{DCB}(t \le t_{DCB})$ (where N is the total number of devices), and the fault current in the DC circuit breaker is given by

$$i_{fault} = i_{C_1} + i_{C_2} + \cdots + i_{CN-1} \le \frac{1}{N-1}I_{DCB} + \frac{1}{N-1}I_{DCB} + \cdots + \frac{1}{N-1}I_{DCB} = I_{DCB}(t \le t_{DCB}) \quad (11)$$

Therefore, when the F2 fault occurs at the line side of VSC, the fault current $i_{F2(vsc)}$ should satisfy (12) after installing the current limiting reactor $L_{F2(VSC)}$.

$$i_{F2(VSC)} \le \frac{1}{N-1}I_{DCB}(t \le t_{DCB}) \quad (12)$$

For DCSST, the fault current $i_{F2(DCSST)}$ should satisfy (13) after installing the current limiting reactor $L_{F2(DCSST)}$.

$$i_{F2(DCSST)} \le \frac{1}{N-1}I_{DCB}(t \le t_{DCB}) \quad (13)$$

3.3. Design Method of Current Limiting Reactor Value

Considering F1 and F2 faults at the same time, the current limiting reactor value should be the higher value between (4) and (12), and is given by

$$L_{(\mathrm{VSC})} = \max[L_{\mathrm{F1(VSC)}}, L_{\mathrm{F2(VSC)}}] \tag{14}$$

For DCSST, the current limiting reactor value is the higher value between (8) and (13), and is given by

$$L_{(\mathrm{DCSST})} = \max[L_{\mathrm{F1(DCSST)}}, L_{\mathrm{F2(DCSST)}}] \tag{15}$$

However, due to the large fault current through DC circuit breaker under the F2 fault, a larger current limiting reactor is needed, which will lead to a larger size of equipment, larger overvoltage, and reduce the dynamic response of the system. It will increase the insulation level of the converter and the recovery time from fault to stability of the system. Compared with the F2 fault, only considering the F1 fault can reduce the value of current limiting reactor and improve the dynamic response, but the F2 fault should be avoided.

4. Simulation

In order to verify the theoretical analysis of the pole-to-pole fault characteristics and the design method of current limiting reactor value for plug-in devices, the simulation was carried out in PSCAD/EMTDC.

4.1. Simulation Modeling

A simulation model of the ±10 kV VSC-DC distribution system in Figure 1 is established in PSCAD/EMTDC. The converter stations, plug-in devices, loads, and line parameters are shown in Tables 1–3, respectively. The converter station is modeled by Thevenin equivalent model, the converter station I is in constant voltage control, and the converter station II is in constant power control. The DC circuit breaker is modeled by time-controlled switch, and the DC cable is modeled by frequency dependent model. The AC load and AC micro-grid are modeled by an equivalent three-phase load of corresponding power, and the DC load and the DC micro-grid are equivalently modeled by the DC current source of the corresponding power. In this simulation model, the time step size of simulation is 5 μs.

Table 1. Parameters of Main Converters.

Device	Converter station I	Converter station II
Capacity	25 MW	25 MW
Submodule number	25	25
Bridge arm reactor	2.5 mH	2.5 mH
Submodule capacitor	31,178 μF	31,178 μF

Table 2. Parameters of Plug-In Devices and Loads.

Device	VSC1	DCSST1	VSC2	DCSST2
Load side voltage	10 kVac	400 Vdc	380 Vac	400 Vdc
Line side capacitor	1500 μF	10,000 μF	1500 μF	10,000 μF
Load type	AC load	DC load	AC micro-grid	DC micro-grid
Capacity	8 MW	4 MW	5 MW	2.5 MW

Table 3. Parameters of DC Cable.

Number	Length/km	Inductance/mH	Resistance/Ω
1	2.3	1.0974	0.106
2	0.9	0.4294	0.0415
3	0.9	0.4294	0.0415
4	0.9	0.4294	0.0415
5	1.0	0.4771	0.0461

4.2. Theoretical Selection and Simulation Verification of Current Limiting Reactors

The DC circuit breaker used in this system can break 10 kA fault current within 5 milliseconds. Therefore, the value of the VSC and DCSST current limiting reactors can be obtained by (14) and (15), respectively. The theoretical results are shown in Table 4 by numerical method in Matlab.

Table 4. Theoretical Calculation Results of Current Limiting Reactor for Per Pole.

Device	L_{F1}/mH	L_{F2}/mH	$L = \max[L_{F1}, L_{F2}]$/mH
VSC1	3	19	19
DCSST1	5	26.5	26.5
VSC2	3	26.5	26.5
DCSST2	5	28	28

That is, the current limiting reactors of 19 mH, 26.5 mH, 20.5 mH, and 28 mH should be installed at each pole of the VSC1, DCSST1, VSC2, and DCSST2 to cooperate with the DC circuit breakers. Compared with F1 faults, more devices discharge through short-circuit points under the F2 fault, resulting in higher fault current flowing through DC circuit breakers. As a result, larger current limiting reactors are needed. In addition, DCSST needs a larger current limiting reactor because of its larger capacitor.

In order to verify the feasibility of the calculation methods of the current limiting reactor, the accuracy of the calculation methods of the fault current should be verified at first. Take VSC1 and DCSST1 as examples, when the F1 fault occurs, the discharge current of VSC1 and DCSST1 are shown in Figure 13.

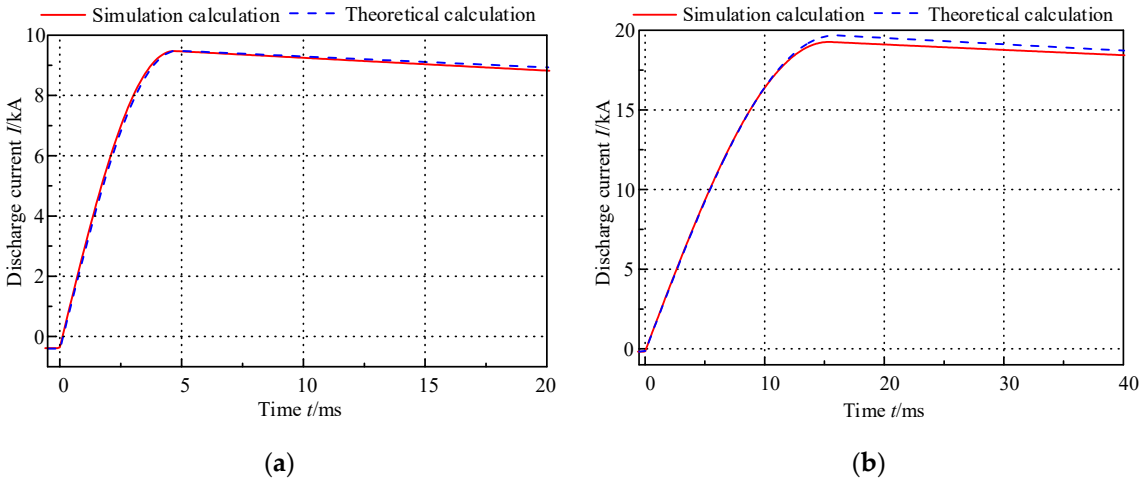

Figure 13. The current waveform under F1 fault by theoretical calculation and simulation calculation: (**a**) VSC1 discharge current and (**b**) DCSST1 discharge current.

Figure 13 shows that the current waveform by theoretical calculation is consistent with the simulation calculation. Therefore, the accuracy of fault current calculation methods under F1 fault can

be proved, and the feasibility of the calculation methods of the current limiting reactor value under F1 fault can be obtained.

For F2 fault, the discharge current of VSC1 and DCSST1 are shown in Figure 14.

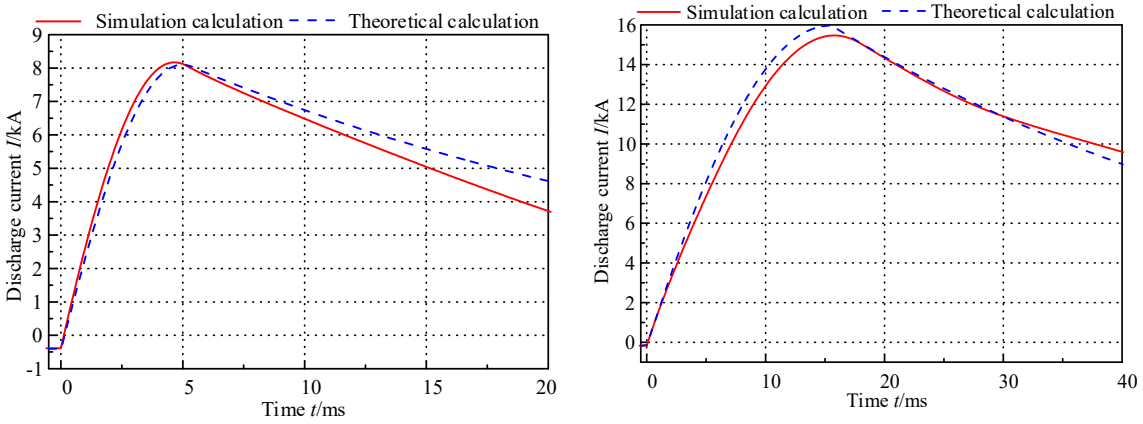

Figure 14. The current waveform under F2 fault by theoretical calculation and simulation calculation: (**a**) VSC1 discharge current when F2 fault occurs in DCSST1 and (**b**) DCSST1 discharge current when F2 fault occurs in VSC1.

When F2 fault occurs, the capacitor of the converters in the system will discharge to the fault point, but due to the difference of discharge time, different devices will charge and discharge each other. However, in order to limit the fault current, it is necessary to limit the fault current in the capacitor discharge stage. Figure 14 shows that in the capacitor discharge stage and the fault current rising stage, the theoretical calculation results are similar to the simulation. Therefore, according to the Equations (9) and (10), the fault current in the capacitor discharge stage under the F2 fault can be calculated, and then the calculation methods of the current limiting reactor value can be obtained.

In addition, in order to verify the current limiting effect of the current limiting reactors by theoretical calculation, the simulation of the F2 fault without current limiting reactors and with current limiting reactors is carried out, and the current waveform obtained by the simulation is shown in Figure 15. The discharge current waveform of DCSST1, VSC2, and DCSST2 during F2 fault in the line side of VSC1 are shown in Figure 16.

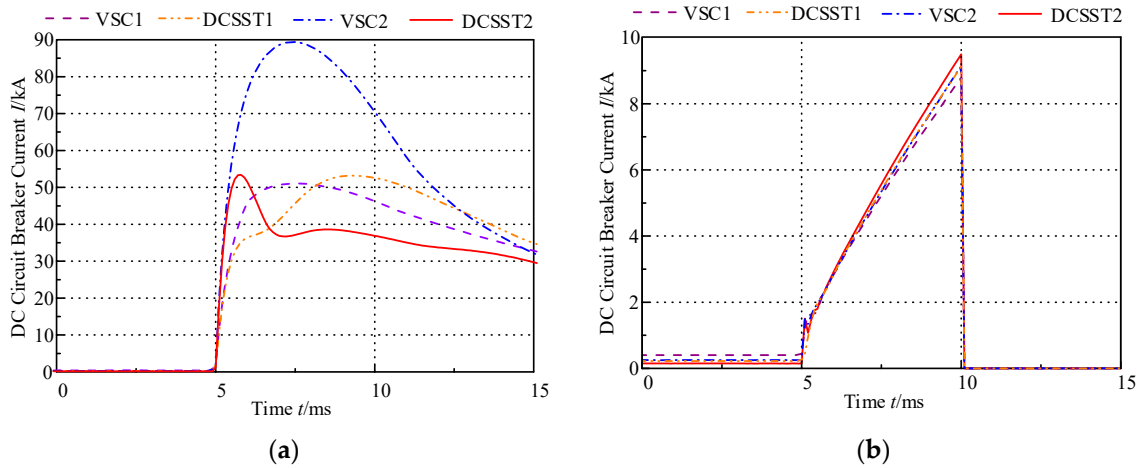

Figure 15. The current of the DC circuit breakers in each device under F2 fault: (**a**) without current limiting reactors and (**b**) with current limiting reactors.

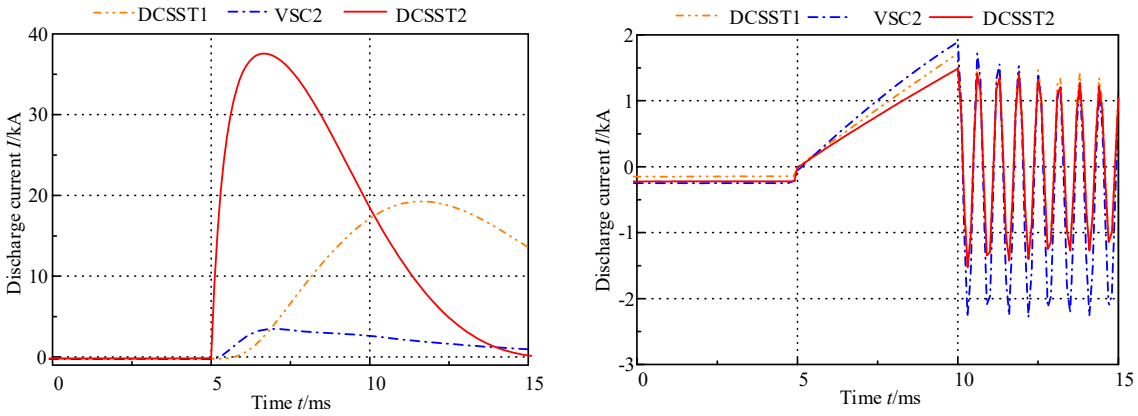

Figure 16. The current of DCSST1, VSC2, and DCSST2 under F2 fault in VSC1: (**a**) without current limiting reactors and (**b**) with current limiting reactors.

Figures 15 and 16 show that the fault current will exceed the breaking capacity of the DC circuit breaker under F2 fault without installing the current limiting reactors, so that the DC circuit breaker cannot isolate the fault. In addition, the closer the device is to the fault point, the higher the discharge current is. After installing the current limiting reactors, the peak value of the fault current in 5 milliseconds is less than 10 kA, which satisfies the breaking capacity of DC circuit breakers. In addition, the discharge current of each plug-in device is less than 2 kA. Therefore, the value of current limiting reactor calculated Formulas (14) and (15) are effective.

However, if F2 fault is considered, the current limiting reactor will be very large, and this is almost impossible to be achieved in an actual project. Compared with the F2 fault, the F1 fault is located at the DC cable termination, so the probability of F1 fault occurrence is higher. If only F1 fault is considered, the value of current limiting reactor can be greatly reduced. The current waveform under F1 fault is shown in Figure 17.

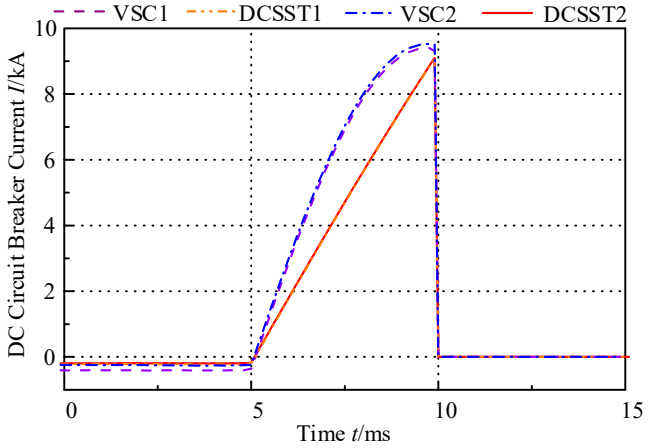

Figure 17. The current of the DC circuit breakers in each device under F1 fault.

Figure 17 shows that after installing the current limiting reactors, the peak value of the fault current in 5 milliseconds is less than 10 kA, which satisfies the breaking capacity of DC circuit breakers. Taking VSC1 as an example, if F2 fault is not considered, the value of limiting current reactor can be reduced by 84.2%. It can not only reduce the area and cost of equipment but can also reduce the overvoltage generated by the limiting current reactor and improve the dynamic response.

5. Conclusions

According to a ±10 kV VSC-DC distribution system, the paper studies the generation mechanism, influencing factors and limiting methods of the pole-to-pole fault current at the line side of plug-in devices. The main conclusions are as follows:

(a) The generation mechanism of F1, F2 and F3 fault current are analyzed theoretically, in which F1 and F2 need to be taken into consideration when designing the current limiting reactors.

(b) The generation mechanism and influencing factors of typical fault current in VSC and DCSST are analyzed theoretically, and the calculation methods of fault current are proposed, such as (1), (2), (5), (6), (9), (10). Also, the current magnitude at different time can be obtained by these calculation methods, so it can provide reference for the setting value of overcurrent protection.

(c) Based on the generation mechanism of fault current and the breaking capacity of the DC circuit breaker, the calculation and selected methods of current limiter reactor value are proposed, such as (4), (8), (12), (13), (14), (15). The size of the current limiting reactor can be determined according to different system parameters and different breaking capacity of the DC circuit breaker. For different breaking capacities of DC circuit breakers, the corresponding current limiting reactor can be obtained by these calculation methods.

(d) The accuracy and reliability of theoretical calculation methods are verified by simulation in PSCAD/EMTDC.

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