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Enhanced Control for Improving the Operation of Grid-Connected Power Converters under Faulty and Saturated Conditions

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Abstract: In renewable energy based systems Grid-Connected Voltage Source Converters (GC-VSC) are used in many applications as grid-feeding converters, which transfer the power coming from the renewable energy sources to the grid. In some cases, the operation of GC-VSC may become unstable or uncontrollable due to, among others: a grid fault or an inappropriate current-power reference, that give rise to fast electrical transients or a saturation of the controller. In this paper, an improved control scheme is proposed to enhance the controllability of GC-VSC in all these situations. This solution consists of two parts, on the one hand a new Proportional-Resonant (PR) controller with anti-windup capability to be used as current controller, and secondly a new current/power reference modifier, which defines the suitable reactive current/power reference to keep the system stable. It is worth to mention that the proposed scheme does not need information about the grid parameters as it only uses the converter current, and the voltage at the capacitors of Inductor-Capacitor (LC) output filter.

Keywords: current control; current reference generation; Low Voltage Ride Through (LVRT); grid connected voltage source converter; renewable resource; Proportional-Resonant (PR) controller

1. Introduction

Two-level three-phase voltage source converters (VSCs) are widely used as grid-feeding inverters, which are controlled resembling a current source in many applications, especially in renewable energy systems, high voltage DC transmission systems and microgrids [1–7], among others. Among linear current controllers, the most extended solutions are those based on using the following reference frames: natural *abc*, synchronous *dq*0 and stationary $\alpha\beta$0. No matter the final selection, the resulting controller for the VSC shall be able to track the reference signal fast and with zero steady-state error, as the current control is the inner and fastest control layer [8,9].

Although synchronous *dq*0 and stationary are mathematically equivalents, using stationary $\alpha\beta$0 reference frame controllers is a very attractive option as it gives rise to a simple digital implementation. In the $\alpha\beta$0 domain, the coordinate transformations are simple and less costly from a computational point of view. Likewise, in this reference frame the cross-coupling terms between control axes are not necessary, as a difference with implementations based on *dq*0 axis [10].

Among linear controllers Proportional-Integral (PI) controllers and Proportional-Resonant (PR) controllers are the most popular ones. The transient and steady state response of PR controllers in the

$\alpha\beta$ stationary frame and PI controllers in the dq synchronous frame have the same performance [11]. However, using PR controllers in the $\alpha\beta$ reference frame give some extra advantages, such as the fact that a single controller is able to control simultaneously the negative and the positive sequences and eliminates the need of using Park transformations, meanwhile its implementation is simple and does not imply a relevant computational cost [12,13].

In the literature, many papers have been published about proportional-resonant controllers, addressing different topics such as different PR topologies, discretization/digital implementation [14–16] and parameters tuning [17–22], among others.

In renewable energy applications, the limitation of the converter's capacity may give rise to the saturation of the integral terms of the controllers and the system can become unstable or uncontrollable. Therefore, using appropriate methods to avoid saturation of integral terms are vital. In linear applications, two solutions can be employed to prevent system uncontrollability: (1) reference modifier; (2) using a controller with anti-windup capability. In [23] a scheme based on a PI controller is used to reduce the reactive current set point to prevent system uncontrollability, but this is too slow and it is not applicable to transient situations. A PR controller with anti-wind up has been proposed in [7,24] which clamps the output of controller in case of the integrator's saturation, however clamping the output give rise to distortions at the output.

Until now, there are no references in the literature proposing a unified and specific scheme to prevent uncontrollability of GC-VSC. In this paper, a new scheme in the stationary reference frame is proposed to address this issue. The proposed scheme includes a reference modifier located in an outer loop, and a PR controller with anti-wind capability in the inner loop. The reference modifier modifies the references to keep the GC-VSC under control measuring the converter current and the voltage at the output filter of the converter. In the proposed PR controller, the output of the controller is always an AC signal without any dc component. In order to show the good performance of this proposal a real grid-connected VSC application is used to implement the proposed controller.

This paper is organized as follows: in Section 2, the description of the development of proposed control scheme is addressed. Section 3 provides validation results to verify the performance of the proposed controller. The conclusion of the work is presented in Section 4.

2. Control Strategy

The schematic of a typical grid connected voltage source inverter is shown in Figure 1. In this case the current reference ($i^*_{\alpha\beta}$) is defined based on the active/reactive power references or the current references that should be injected to the grid. In the current loop, the PR controller is tuned to ensure zero steady error and a fast transient response. In the schematic of Figure 1, in order to enhance the dynamic response, a feedforward of the voltage is used. This voltage feedforward, which is multiplied by the coefficient k_f, improves the transient response and decrease startup current [25], but, on the other hand, it makes the loop more sensitive to distortions that may affect the voltage.

The schematic of the outer loop block is shown in Figure 2, where the current reference in the stationary reference frame is obtained using the current/power set points and the PCC voltage using the following expression:

$$\begin{bmatrix} i^*_{\alpha+} \\ i^*_{\beta+} \end{bmatrix} = \frac{1}{\sqrt{v^2_{\alpha1+}+v^2_{\beta1+}}} \begin{bmatrix} v_{\alpha1+} & v_{\beta1+} \\ v_{\beta1+} & -v_{\alpha1+} \end{bmatrix} \begin{bmatrix} I^*_{a+} \\ I^*_{r+} \end{bmatrix} = T^+ \begin{bmatrix} I^*_{a+} \\ I^*_{r+} \end{bmatrix}, \quad (1)$$

$$\begin{bmatrix} i^*_{\alpha-} \\ i^*_{\beta-} \end{bmatrix} = \frac{1}{\sqrt{v^2_{\alpha1-}+v^2_{\beta1-}}} \begin{bmatrix} v_{\alpha1-} & v_{\beta1-} \\ v_{\beta1-} & -v_{\alpha1-} \end{bmatrix} \begin{bmatrix} I^*_{a-} \\ I^*_{r-} \end{bmatrix} = T^- \begin{bmatrix} I^*_{a-} \\ I^*_{r-} \end{bmatrix}, \quad (2)$$

where, $I^*_{a\pm}$ and $I^*_{r\pm}$ are the active and the reactive components of the converter current set points in the positive/negative reference frame respectively. In this paper a Dual Second Order Generalized Integrator Frequency Locked Loop (DSOGI-FLL), is used for estimating the magnitude of the

symmetrical components of the voltage at the PCC. This synchronization system was proven accurate and fast under unbalanced and distorted conditions of the electrical network [26,27].

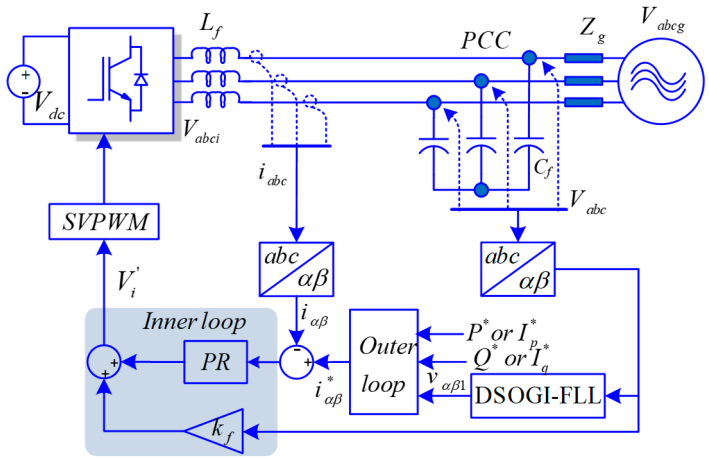

Figure 1. Schematic grid connected converter.

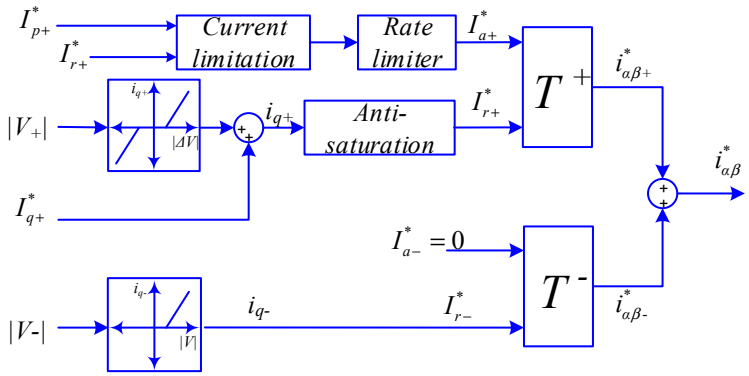

Figure 2. Schematic of the outer loop including the proposed anti-saturation scheme to generate the current reference.

According to standards, the converter should inject reactive currents to support the grid during faults. In grid codes, as the VDE-AR-N 4120 [28], the reactive current reference $i_{q\pm}$ is defined based on the PCC voltage drop/rise multiplied by the droop coefficient $k_{v\pm}$. As in many applications, a dead-band is considered in this case. The value of I^*_{r+} is obtained from the reactive current command I^*_{q+} plus i_{q+}. The I^*_{a-} equals to zero according to standard and the I^*_{r-} is equal to i_{q-}. The contribution of GC-VSC to the PCC voltage support is mathematically written in (3) and (4) according to VDE-AR-N 4120 [23,28].

$$\begin{cases} i_{q+} = 0 & |\Delta|V_+|| < V_{band+} \\ i_{q+} = k_{v+}(\Delta|V_+| - V_{band+}) & \Delta|V_+| > V_{band+} \\ i_{q+} = k_{v+}(\Delta|V_+| + V_{band+}) & \Delta|V_+| < -V_{band+} \end{cases} \tag{3}$$

$$\begin{cases} i_{q-} = 0 & |V_-| < V_{band-} \\ i_{q-} = k_{v-}(|V_-| - V_{band-}) & |V_-| > V_{band-} \end{cases} \tag{4}$$

where $V_{band\pm}$ is the threshold voltage in which GC-VSC has to work in voltage supporting mode by injecting reactive current to the PCC. Also, $\Delta|V_+|$ and $|V_-|$ are equal to $1-|V_+|$ and $|V_-|$, in per unit, respectively.

In high power converters the current/power reference does not change following a step, but the set point variations track normally a ramp. In Figure 2, the rate limiter is used to implement these

set point changes [25]. The current limiter is used to reduce the active current reference in case of grid faults when the reactive current is increased to support the grid voltage [23]. Depending on the application, the country and the technology this rate limiter may be different.

2.1. Saturation and Uncontrollability Scenarios of a GC-VSC

To show how the VSC can lose the controllability, a VSC is modeled as a controllable voltage source V_i which is connected to the PCC through a LC filter, as shown in Figure 3. The grid is simplified as a voltage source, V_g, connected in series with an impedance Z_g. Only the voltage at the PCC and the inverter current are measured to control the system. In the case of the inductor of the LC filter, the resistive part is neglected as its value is not significant compared to the inductive part. Moreover, the inherent resistor in a real application would introduce damping, what benefits the performance. Therefore, avoiding the resistor makes the analysis even more restrictive and hence the proposed method should perform even better. In this case, the GC-VSC is controlled within the following operating boundaries:

(1) Using a space vector modulation the linear control range of the output fundamental component can be extended a 15%. However, for a six-step square-wave controlled inverter, the magnitude of the output fundamental voltage is equal to $(2/\pi)\ V_{dc} = 0.6366\ V_{dc}$. Increasing the output voltage of a PWM-controlled inverter from $0.575\ V_{dc}$ to the limit of $0.6366\ V_{dc}$, is done by entering to the nonlinear region. The region of operation between the loss of linear control (m = 1.15) and complete loss of control (uncontrollability) (m = 1.27) is called the over-modulation region. When over modulation occurs, the modulation index m exceeds the triangle wave in modulator. Note that when m > 1, or m > 1.15 as appropriate, the actual resultant fundamental component does not linearly follow m, and the controller is saturated. Consequently, the shape of the output voltage waveform is only partially under control. Since the modulator effectively loses control of the output waveform during the saturation intervals, the output waveform becomes progressively distorted and includes low-frequency harmonics [29]. Therefore, the amplitude and phase of V_i is determined by the input voltage of the switching modulator, the switching method and the dc bus voltage V_{dc}. The peak of V_i cannot be higher than $0.6366\ V_{dc}$ for any switching methods. When an inverter works in grid-supporting mode or grid-feeding mode, the inverter voltage has to be higher than the PCC voltage to deliver reactive power to the grid. To inject reactive power, if the input of switching modulator is higher than triangle wave, the current controller becomes saturated, hence the inverter becomes uncontrollable and the waveforms of the injected current gets distorted.

(2) The GC-VSC current has to be under the semiconductor's current rating. In transient conditions, as for instance: power/current reference sudden change, inverter's start-up or when there is a grid fault, the inverter current may experience some overshoots, due to the delay of the current controller, and the wind-up effect at the integrators of the controllers. However, a high current overshoot might give rise to an undesired converter trip or to a critical damage of the semiconductors.

(3) The GC-VSC should help the grid in case of grid faults according to the Low Voltage Ride Through (LVRT) curve. Typically the reactive current coefficient $k_{v\pm}$ is higher than 2 [23,28]; therefore the active current should be set to zero under severe grid faults to keep the VSC current under the rated value.

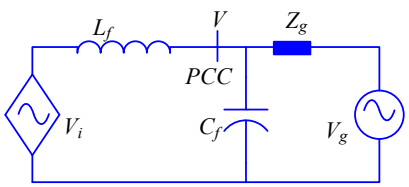

Figure 3. Simplified model of grid-connected inverter.

As it can be seen in Figure 3, the output voltage of the inverter, namely V_i, can be decomposed into its symmetrical components. In this case, just the positive and negative sequence will be considered, as it is a three-phase three-wire system and thus zero-sequence circuit analysis is not required due to the absence of zero sequence current components. For the positive sequence, the active current, responsible of the active power delivery and the positive sequence voltage are in phase, but the reactive current is shifted 90 degrees with respect to the positive sequence voltage. Regarding the negative sequence, only reactive current is injected to the PCC according to the VDE-AR-N 4120. The negative sequence reactive current is shifted 90 degrees with respect to the negative sequence voltage. In Figures 4–9, the phasor diagrams and numerical results of GC-VSI are shown based on several simulations. The values of voltages and currents are captured from simulation results.

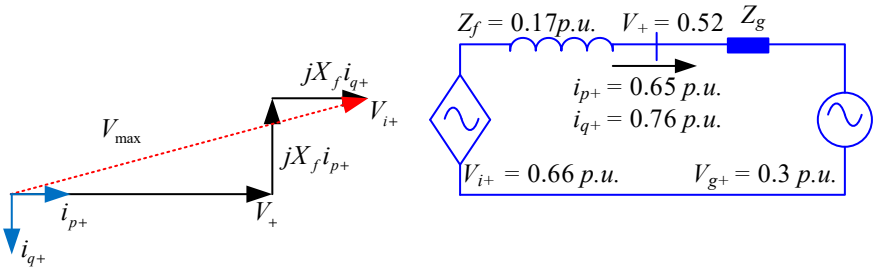

Figure 4. Vector representation of voltages and currents of GC-VSC working at normal grid conditions or balanced voltage changes while injecting reactive power.

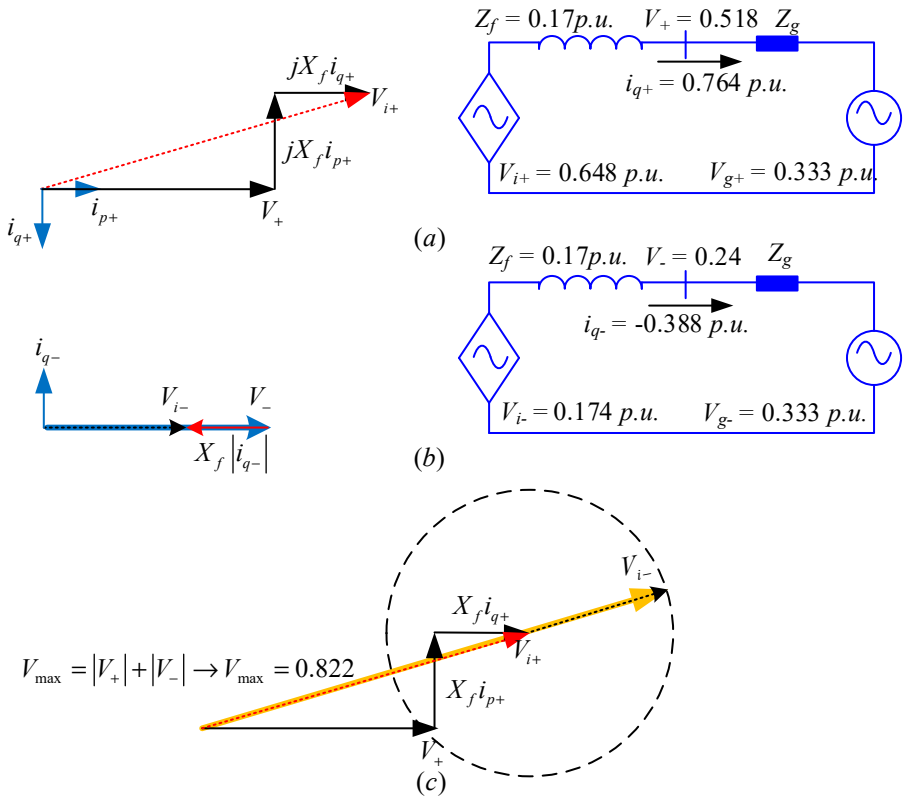

Figure 5. Vector representation of voltages and currents GC-VSC when there is an unbalanced voltage sag. (**a**) Positive sequence. (**b**) Negative sequence. (**c**) Inverter voltage in the worst case.

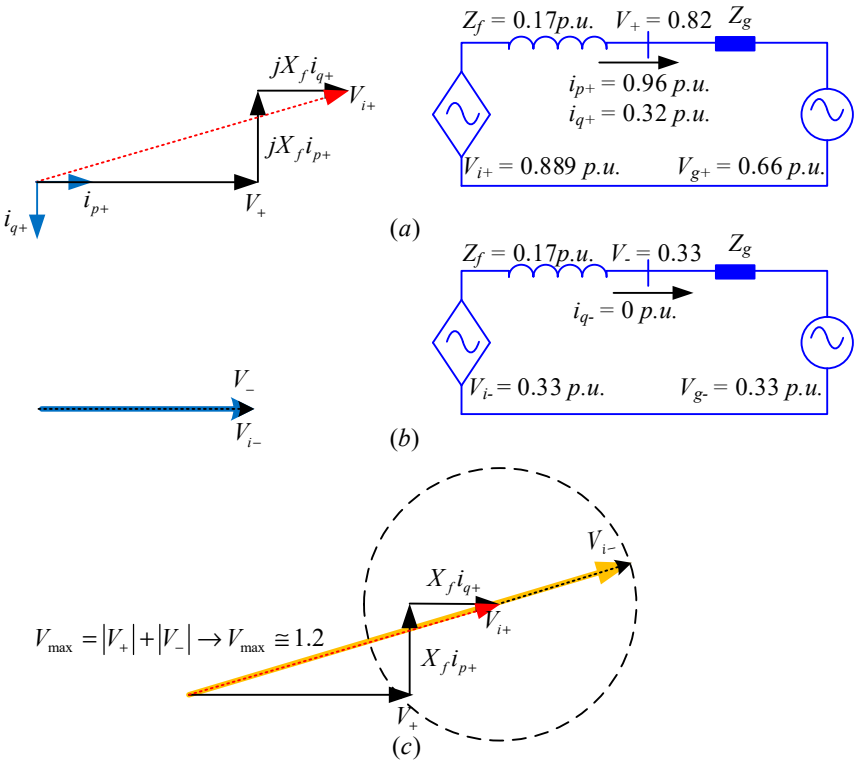

Figure 6. Vector representation of voltages and currents GC-VSC for unbalanced voltage sag without injecting negative sequence current during the fault. (**a**) Positive sequence. (**b**) Negative sequence. (**c**) Inverter voltage in the worst case.

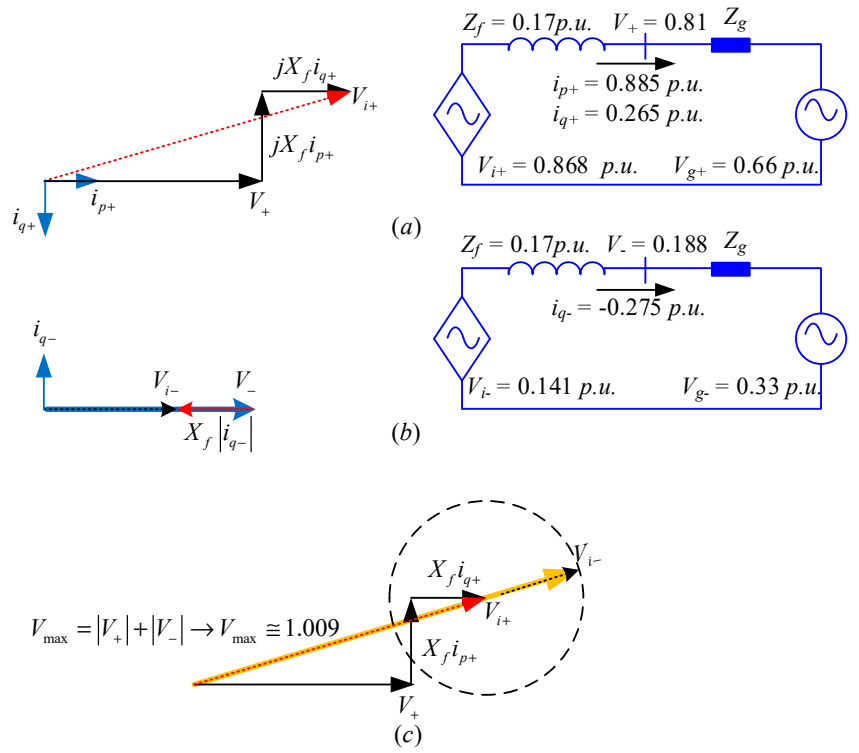

Figure 7. Vector representation of voltages and currents of GC-VSC for unbalanced one phase 100% voltage sag injecting negative sequence current during the fault. (**a**) Positive sequence. (**b**) Negative sequence. (**c**) Inverter voltage in worst case.

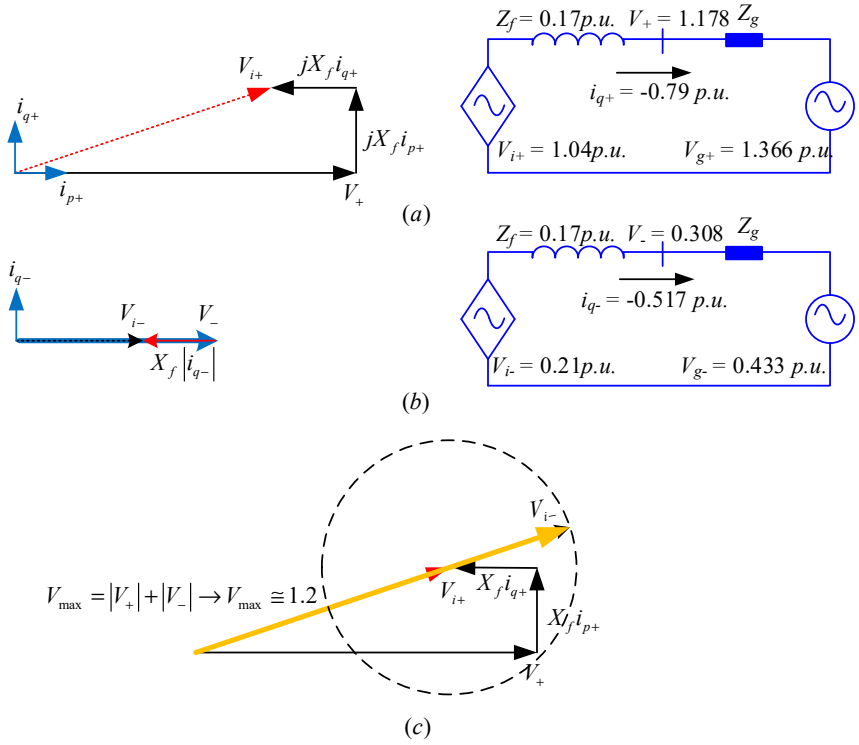

Figure 8. Vector representation of voltages and currents of GC-VSC for voltage swell. (**a**) Positive sequence. (**b**) Negative sequence. (**c**) Inverter voltage in the worst case.

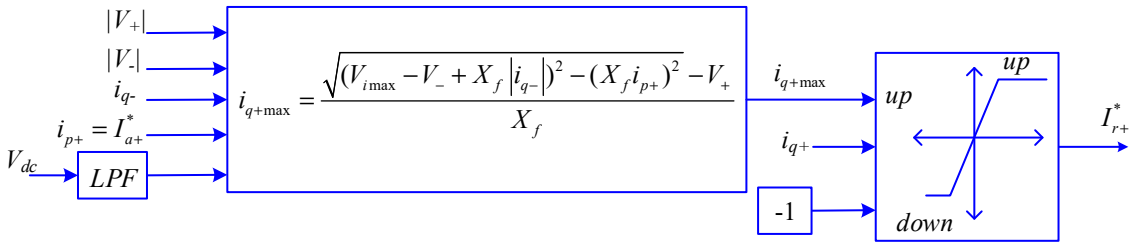

Figure 9. Anti-saturation scheme considering positive and negative sequence current references.

Figure 4 shows the representation of the positive sequence vector of the voltage and the current in case of balanced voltage sags, when the delivery of reactive power to the grid is required. For balanced voltages, the amplitude of the negative sequence in the grid voltage is zero. Therefore, it is only necessary to analyze the positive sequence performance. However, as it can be deducted from Figure 4, for injecting reactive power to the grid, the amplitude of the inverter voltage must be bigger than the voltage at the PCC. Generally, in the case of balanced voltage sags, there is no difficulty to inject reactive power to grid because the PCC voltage decreases while the DC bus voltage is constant. Hence, the controller will not saturate because of the lack of control action. As an example, the amplitude of currents and voltages for three-phase 70% voltage sag are shown in Figure 4, where the inverter voltage is lower than 1.15 p.u. and anti-saturation is not necessary. However, under normal conditions, the controller can be saturated when the inverter injects reactive power to the grid. In these conditions, the implementation of an effective reference modifier scheme is essential to limit the reactive current set point.

The voltages and currents vector representation considering the occurrence of an unbalanced voltage sag are shown in Figure 5. In addition, the numerical values of two-phase 100% voltage sags are depicted in this figure. In this faulty scenario, in order to improve the positive sequence voltage at

the PCC, the inverter should inject reactive power. For injecting reactive power to the PCC (capacitive mode), the positive sequence amplitude of the inverter voltage must be higher than the PCC voltage. On other hand, the negative sequence reactive current go through the inverter until reaching the PCC. Therefore, the voltage of the inverter contains both positive and negative sequence components. As in the previous case, by making the vector addition of the inverter's voltage components in Figure 5a, it can be seen that the probability of losing controllability is low.

The numerical results and the vector diagrams of a single-phase voltage sag without injecting negative sequence currents are shown in Figure 6. As it can be seen in this plot, if the positive sequence reactive current is bigger than 0.32 p.u., then the controller will be saturated. In fact, the system is working at the border of its controllability, as it can be seen in Figure 6.

The previous case depicted in Figure 6 is repeated again in Figure 7; but in this case, the negative sequence current is injected. As it can be seen, the maximum value of the inverter voltage is reduced from 1.2 p.u. to 1 p.u. In addition, the active positive sequence current is reduced to 0.885 if compared to Figure 6, due to the converter's current limitation.

The vector diagrams and simulation results of the inverter in case of voltage swell are shown in Figure 8. The inverter, by delivering inductive reactive power, contributes to support the operation of the grid and to keep PCC voltage in the standard range. In this case, the value of reactive current is determined based on the PCC voltage deviation multiplied to $k_{v\pm}$. For i_{q+} and i_{q-} equal to -0.79 and -0.517 p.u., the V_{i+} and V_{i-} have to 1.04 p.u. and 0.21 p.u. respectively. Therefore, the inverter has to produce a V_i around 1.25 p.u., which is quite the controllability limit. In these conditions, the controller will become saturated because the value of reactive current (i_{q+}) is not suitable, so the value of i_{q+} needs to be modified and limited by the saturation scheme.

2.2. Development of the Proposed Anti-Saturation Scheme

In this section, a new analytical anti-saturation scheme will be proposed. As a difference with other techniques, this proposal does not need information about the equivalent grid impedance (Z_g) or the grid voltage (V_g) and permits the converter to remain stable at normal and faulty situations. The importance of this anti-saturation block is once the vector diagrams of currents and voltages in different conditions were reviewed in the previous section.

In Figure 3 by writing the KVL, the inverter positive sequence voltage can be found as:

$$\begin{aligned} &V_{i+} = V_+ + jX_f i_{q+} + jX_f i_{p+} \\ &\rightarrow |V_{i+}| = \sqrt{(V_+ + X_f i_{q+})^2 + (X_f i_{p+})^2} \end{aligned} \tag{5}$$

In the negative sequence domain, only reactive current is injected to the PCC according to VDE-AR-N 4120. The negative sequence reactive current is shifted 90 degrees with respect to the negative sequence voltage. The amplitude of the inverter's voltage in the negative sequence can be written as:

$$\begin{aligned} &V_{i-} = V_- + jX_f i_{q-} \\ &\rightarrow |V_{i-}| = V_- - X_f |i_{q-}| \end{aligned} \tag{6}$$

where the value of i_{q-} can be positive or negative depending on the transformations, but the Equation (6) is correct for any value of i_{q-}. The negative sequence voltage rotates at twice the frequency with respect to the positive sequence voltage. In the worst case, the maximum value of the inverter voltage can be found when the positive sequence voltage and negative sequence voltage have the same direction as shown in Figures 4–8. Therefore:

$$\begin{aligned} &V_{i\max} = |V_{i+}| + |V_{i-}| \\ &\rightarrow V_{i\max} = \sqrt{(V_+ + X_f i_{q+})^2 + (X_f i_{p+})^2} + V_- - X_f |i_{q-}| \end{aligned} \tag{7}$$

For an inverter with specific DC voltage, the maximum phase voltage can be found as:

$$V_{i\max} = m_{\max}\frac{V_{dc}}{2} = \frac{V_{dc}}{\sqrt{3}} \tag{8}$$

Hence, the maximum reactive current can be found by substituting (8) into (7):

$$i_{q+\max} = \frac{\sqrt{(V_{i\max} - V_- + X_f|i_{q-}|)^2 - (X_f i_{p+})^2} - V_+}{X_f} \tag{9}$$

The scheme of the anti-saturation principle written in (9) is shown using a block diagram in Figure 9. In Figure 9, the value of i_{q-} is found by multiplying k_{v-} by the negative sequence voltage, meanwhile i_{q+} is related to the reactive power set point and droop function of the PCC's positive sequence voltage. The DC bus voltage measurement is filtered in order to remove ripples and high frequency noises. In (9) and Figure 9, i_{p+} is equal to I^*_{a+}.

The scheme in Figure 9 is proposed to find the maximum value of reactive current reference to prevent saturation of the controller. In many systems, only the control of the active and reactive power in the positive sequence is important and the current reference can be found from the following equation in Figure 1 [15]:

$$\begin{bmatrix} i^*_{\alpha+} \\ i^*_{\beta+} \end{bmatrix} = \frac{1}{v^2_{\alpha 1+}+v^2_{\beta 1+}} \begin{bmatrix} v_{\alpha 1+} & v_{\beta 1+} \\ v_{\beta 1+} & -v_{\alpha 1+} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} \tag{10}$$

In this section, a new scheme is proposed to determine the maximum of reactive power reference to prevent from controller saturation.

Considering the diagram of Figure 3, the apparent power injected by the inverter to the PCC can be written as:

$$\begin{aligned} S &= (v_\alpha + jv_\beta)\overline{(i_\alpha + ji_\beta)} = (v_\alpha + jv_\beta)\overline{(\frac{v_{\alpha i}-v_\alpha+j(v_{\beta i}-v_\beta)}{jX_f})} \\ &= \frac{(v_\alpha v_{\beta i}-v_\beta v_{\alpha i})}{X_f} + j\frac{\left(v_\alpha v_{\alpha i}+v_\beta v_{\beta i}-(v^2_\alpha+v^2_\beta)\right)}{X_f} \end{aligned} \tag{11}$$

Figure 10 can be used to simplify (11). According to Figure 10, the relationships between voltages can be described by:

$$\begin{aligned} V_{\alpha\beta} &= \sqrt{v^2_\alpha + v^2_\beta}, v_\alpha = V_{\alpha\beta}\cos\theta_1, v_\beta = V_{\alpha\beta}\sin\theta_1 \\ V_{\alpha\beta i} &= \sqrt{v^2_{\alpha i} + v^2_{\beta i}}, v_{\alpha i} = V_{\alpha\beta i}\cos\theta_2, v_{\beta i} = V_{\alpha\beta i}\sin\theta_2 \end{aligned} \tag{12}$$

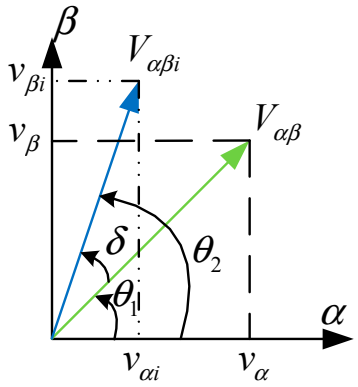

Figure 10. Vector representation of voltages of Figure 3.

Substituting (12) into (11), yields:

$$S = \frac{V_{\alpha\beta}.V_{\alpha\beta i}}{X_f}, \tag{13}$$

$$P = \frac{V_{\alpha\beta}.V_{\alpha\beta i}\sin\delta}{X_f} = S\sin\delta, \tag{14}$$

$$Q = \frac{\left(V_{\alpha\beta}V_{\alpha\beta i}\cos\delta - (V_{\alpha\beta})^2\right)}{X_f} = S\cos\delta - \frac{{V_{\alpha\beta}}^2}{X_f}, \tag{15}$$

Squaring the equations of P&Q in (14) and (15) and rearranging,

$$P^2 + (Q + \frac{{V_{\alpha\beta}}^2}{X_f})^2 = S^2(\sin\delta)^2 + S^2(\cos\delta)^2 = S^2 \rightarrow Q = \sqrt{S^2 - P^2} - \frac{{V_{\alpha\beta}}^2}{X_f} \tag{16}$$

The maximum apparent power injected by the inverter to the PCC can be found by substituting (8) into (13):

$$S_{\max} = \frac{V_{\alpha\beta}.V_{i\max}}{X_f} \tag{17}$$

Therefore, the maximum reactive power can be found by combining (17) and (16):

$$Q_{\max} = \sqrt{(\frac{V_{\alpha\beta}.V_{i\max}}{X_f})^2 - P^2} - \frac{V_{\alpha\beta}^2}{X_f},\ V_{\alpha\beta} = |V| \tag{18}$$

The final anti-saturation scheme based of this analytical method is shown in Figure 11.

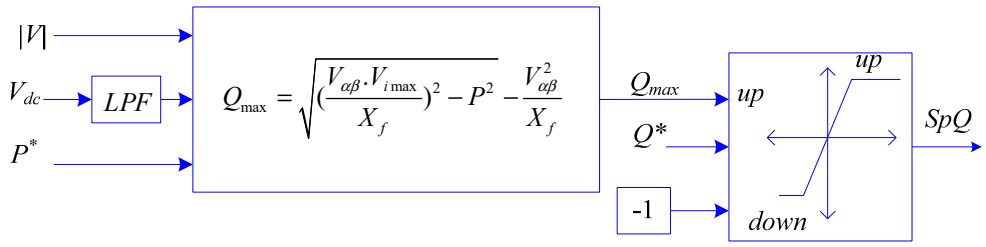

Figure 11. Anti-saturation scheme considering active and reactive power references.

2.3. PR Controller with Anti-Windup Capability

In fact, the anti-wind up of the PR controller and the anti-saturation scheme should work complementary together. In the transient case, the anti-windup block of the PR controller limits the input of the switching modulator and prevents the saturation of the integral terms of the PR controller. In steady state, the anti-saturation reference modifier reduces the reactive current/power reference and prevents the saturation of the controller.

The PR controller can be expressed as:

$$C_i(s) = PR = K_p + \frac{2\omega_c K_i s}{s^2 + 2\omega_c s + \omega_o^2}, \tag{19}$$

where K_p, K_i, ω_o and ω_c are the proportional gain, the resonant gain, the resonant frequency and the resonant bandwidth, respectively. The PR controller is used to ensure zero steady-state error and a fast dynamic response. Because of limitations in practical implementations an ideal resonant controller (ω_c = 0) cannot be used. The frequency response of PR controller, at frequencies higher than or lower than the resonant frequency all the plots converge to the 20 dB per decade asymptotic response

regardless of the value of ω_c. The major difference between the different plots is the increasing peak amplitude at the resonant frequency (ω_o) for smaller values of ω_c. The infinite gain benefit of the ideal resonant term only happens at the resonant frequency and any perturbation will lead to a reduction of the generated gain. Hence, the resonant regulator is potentially sensitive to the alignment between the regulator's resonant frequency (ω_o) and the fundamental frequency of the grid. To solve this issue, instantaneous estimation of frequency from FLL is fed to PR controller and the value of resonant bandwidth is set 2 rad/s in this paper. The implemented PR controller based on two integrators is shown in Figure 12.

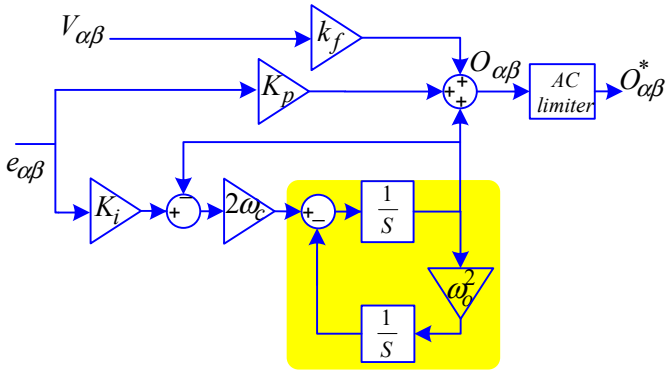

Figure 12. Block diagram of PR controller with two integrators.

The output of the PR controller (input switching modulator (SM)) must be lower than the specific value $O_{\max}$, otherwise there will be over modulation. In over modulation, the switching frequency is reduced and the waveforms at the inverter's output are distorted [29]. The proposed AC limiter (ACL) to limit the input of SM can be expressed as:

$$\begin{cases} \left|O_{\alpha\beta}\right| = \sqrt{O_\alpha^2 + O_\beta^2} \\ O^*_{\alpha\beta} = O_{\alpha\beta}, \quad \left|O_{\alpha\beta}\right| < O_{\max} \\ O^*_{\alpha\beta} = \frac{O_{\max}}{\left|O_{\alpha\beta}\right|} out_{\alpha\beta}, \quad \left|O_{\alpha\beta}\right| > O_{\max} \end{cases} \tag{20}$$

It is worth mentioning that in common limiters the output is clamped in case of wind up. However, by the proposed method, the input of SM has no clamp and it is always sinusoidal. The value of $O_{\max}$ is chosen based on the switching method.

When a limiter inhibits the output of a controller, any integrators within the controller may experience wind-up, as it can be concluded from Figure 12. In this paper, a new PR controller with anti-windup capability is proposed in Figure 13. The difference between the controller's output and the AC limiter (ACL) lays mainly on the feedback signal to compensate the inputs of the integrators. In this controller, the ACL is used inside of anti-wind-up as the main block. The maximum available output of the PR controller $O_{\max}$ is the main important variable in the anti-windup strategy, which should be selected based on V_{dc}. The value of $O_{\max}$ ($V_{i\max}$) depends on the switching method of inverter according to (8). The $V_{i\max}$ is needed for two parts: anti-saturation scheme and anti-windup of PR controller. For anti-saturation scheme is set $V_{dc}/\sqrt{3}$ to prevent uncontrollability. For PR controller with anti-windup, $m_{\max}$ is chosen based on the switching method according to Equations (21) and (22). Therefore, the allowed maximum value of for three different switching methods: Sinusoidal pulse width modulation (*SPWM*), Space Vector Pulse Width Modulation (*SV-PWM*) and Square wave modulation can be found from:

$$O_{\max} = V_{i\max} = \frac{V_{dc}}{2} - \frac{t_{dead}}{Ts} V_{dc}, \; m_{\max} = 1, SPWM \tag{21}$$

$$O_{\max} = V_{i\max} = \frac{V_{dc}}{\sqrt{3}} - \frac{t_{dead}}{Ts} V_{dc},\ m_{\max} = \frac{2}{\sqrt{3}}, SVPWM \tag{22}$$

$$O_{\max} = V_{i\max} = \frac{2V_{dc}}{\pi} - \frac{t_{dead}}{Ts} V_{dc},\ Square\ wave\ \text{modulation} \tag{23}$$

where t_{dead} and Ts are the switching dead time and the switching period, respectively.

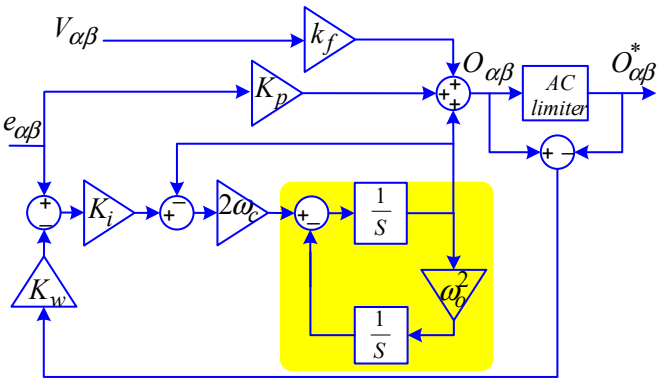

Figure 13. Block diagram of proposed PR controller with anti-wind-up capability.

3. Real Time Simulation Results

In order to test the performance of the proposed controller a Typhoon HIL 600 (Typhoon HIL GmbH, Zurich, Switzerland) has been used to emulate the converter and the grid in real time. The proposed control has been implemented in a TI DSP28335 (Texas Instruments Inc., Dallas, TX, USA) hosted in a controller box that includes the acquisition layer and the digital outputs that would take the signals from the sensors and provide the pulses to the inverter. In this way, not only the proposed controller is tested under realistic conditions but also its implementation is made in a commercial platform.

The schematic and the parameters of 4MVA GC-VSC are shown in Figure 14 and Table 1, respectively. The GC-VSC consists of an inverter bridge with six IGBTs, while the grid-side filter consist of a three-phase inductor with a parallel capacitor, as shown in Figure 14. The nominal dc-link voltage of the inverter is 1150 V DC. The GC-VSC is connected to the grid through a Dyn1 30/0.69 kV three-phase transformer with a 6% impedance. The maximum acceptable inverter current $I_{\max}$ is 7200A (1.5211 p.u.) and $V_{i\max}$ is considered $V_{dc}/\sqrt{3}$ (1.1785 p.u.). The SCR of grid from high voltage side of transformer and X/R of grid impedance are chosen to be 5 and 7, respectively.

The tuning procedure for the current controller parameters (K_p, K_i and k_f) is the one described in [25]. In this study case $V_{band\pm}$ in (3) and (4) is considered to be 0.1 p.u. and also the droop coefficients $k_{v\pm}$ have to be higher than 2 according to VDE-AR-N 4120.

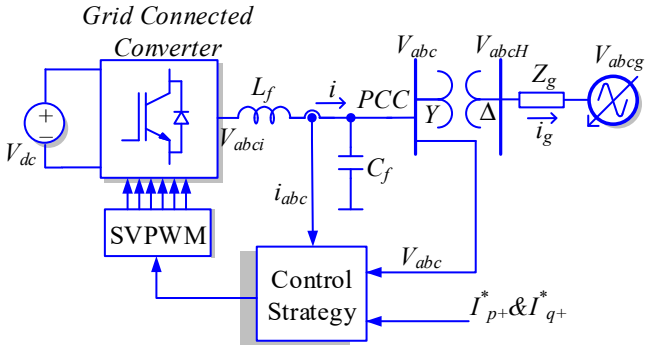

Figure 14. Schematic of the validation layout.

Table 1. GC-VSC Parameters.

Variable	Value	Variable	Value
V (V_{rms})	690	C_f (μF)	1000
S_{NOM} (MVA)	4	f_O (Hz)	50
V_{dc} (V)	1150	f_S (kHz)	2
L_f (μH)	65	SCR	5

The analysis will be performed in two steps: in the first one the operation of the PR controller with anti-windup will be tested. In a second stage, the capability and operation of the entire proposed scheme including reference modifier and PR controller with anti-windup will be tested. In this regard, it is worth to mention that the Real Time Simulator is an essential device as it permits to emulate all kind of scenarios, which will be almost impossible to find in a conventional experimental setup.

3.1. Test of the PR Controller with Anti-Windup Capability

In this section, only the operation of the PR controller is considered and the reference modifier is not employed. In order to show the performance of the PR controller a validation scenario is defined where the reference modifier, which is a part of the proposed scheme (anti-saturation), is not enabled. In this scenario we can show how the performance of the PR controller with the anti-wind up is able to prevent the saturation of the integrators. The plots in Figure 15 gathers the obtained results where I^*_{a+} is set to 0.5 p.u. and I^*_{r+} changes from 0, at t = 0.24 s, to 0.6 p.u. at t = 0.3 s.

Figure 15a shows the results obtained from a typical PR controller. As it is proven, the controller is saturated when the reactive current set point I^*_{r+} is higher than 0.5 p.u. and it cannot track the reference current. It is evident from Figure 15a that a PR controller without anti-windup cannot track the current reference after decreasing I^*_{r+} at t = 0.3 s and the system become unstable due to the saturation of the integrators.

The results of a conventional PR controller [7] with anti-windup are shown in Figure 15b. It can be observed that the system is stable after reducing I^*_{r+} at t = 0.3, because the anti-windup prevents the saturation of the integrators. However, when I^*_{r+} increases, the input of the switching modulator is cropped and the quality of injected current is declined.

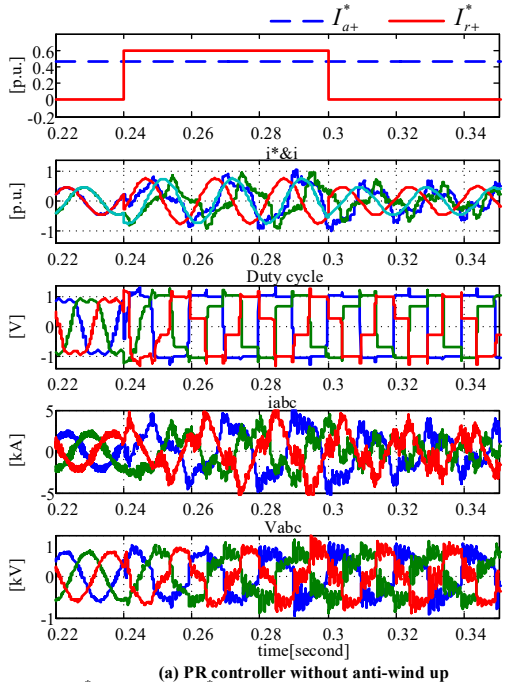

Figure 15. *Cont.*

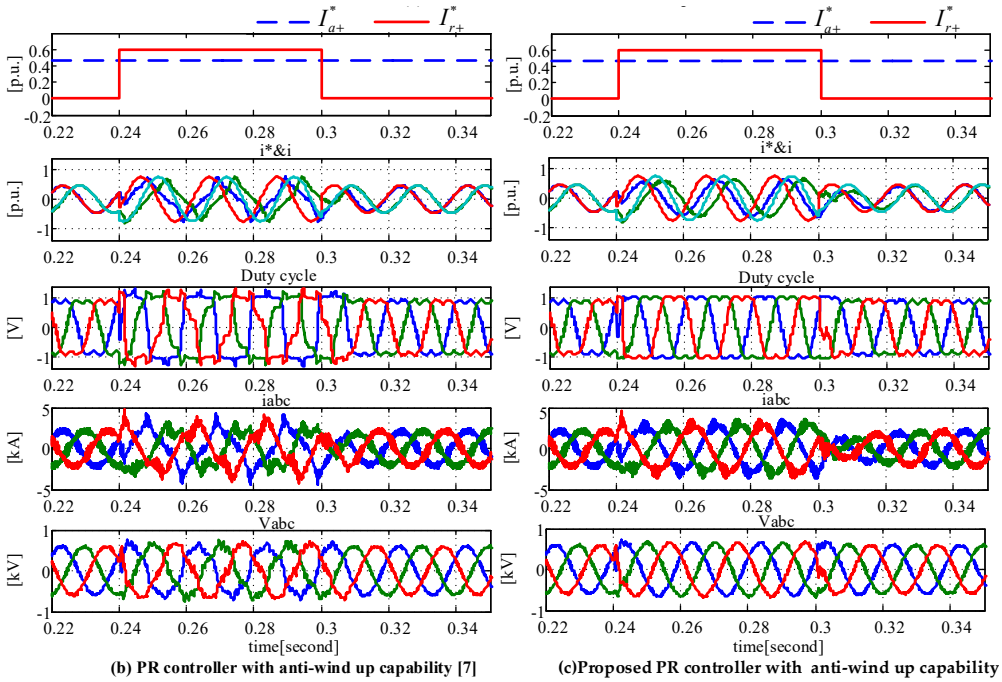

Figure 15. The Real Time Simulation results of inverter with different PR controller for SCR = 5. From top to bottom: in first figure active and reactive current references; in second figure actual and reference currents in $\alpha\beta$ axes; in third figure duty cycle; and in fourth figure converter current and in fifth figure PCC voltage.

Finally, the performance of the proposed PR controller of this paper with anti-wind-up capability are shown in Figure 15c. It is evident that this scheme prevents from saturation integrators and the system become stable after decreasing I^*_{r+}. Also, during the period where uncontrollability may arise, from t = 0.24 s until t = 0.3 s, the injected current is almost sinusoidal thanks to the proposed AC limiter.

3.2. Test of the Entire Proposed Scheme

In this section, some situations are considered where the whole proposed scheme has been implemented in order to prevent uncontrollability issues.

First, a grid with V_{ag} = 0.5 p.u., V_{bg} = 1.8 p.u. and V_{cg} = 1.8 p.u. is considered. It worth to mention that without anti-saturation the system becomes unstable. The results for SCR = 5 are shown from Figures 16–18, where the voltage fault happens from t = 0.25 s until t = 0.4 s.

As shown in Figure 16, when the voltage fault occurs at t = 0.25 seconds, the following actions are performed: (1) Positive sequence reactive current reference becomes negative value -0.45 p.u. according to the VDE-AR-N 4120 for grid supporting. However, this value is not suitable and it should be reduced more for stabilizing of the control system. (2) The anti-saturation scheme reduces positive sequence reactive current set point to -1 p.u. to prevent system uncontrollability. (3) The negative sequence reactive current set point is increased from zero p.u. to 0.5 p.u. to decrease the negative sequence voltage at the PCC. (4) The positive sequence active current set point is reduced to zero to limit the converter's current.

It can be seen from Figure 16 that the duty cycle is lower than 1 during the fault, due to the action of the anti-saturation scheme.

The final set point of the active and the reactive current in the positive sequence is shown in Figure 17, where I^*_{a+} and I^*_{r+} are zero and -1 during voltage fault, respectively.

Figure 18 shows the voltage and current waveforms at both, PCC and grid side, for the first scenario. In this case, at the high voltage side of the transformer a severe fault has occurred, as the voltage of two phases increases an 80% and the third phase voltage is reduced 50%. However, it is

clear that the proposed scheme forces GC-VSC to inject a suitable current in order to support the grid voltage. Therefore, the voltage at the PCC is almost balanced and compensated compared to the one measured at the high voltage side of the transformer.

The outer loop generates the current reference in the stationary reference frame (two sinusoidal current references) based on the positive and negative sequence of the PCC voltage and the active and reactive current references. The resulting current reference is followed with a zero-steady state error and a suitable transient response, as it can be seen in Figure 18. It is worth to remark that the current of the converter has always been below the maximum value, hence within safety margins.

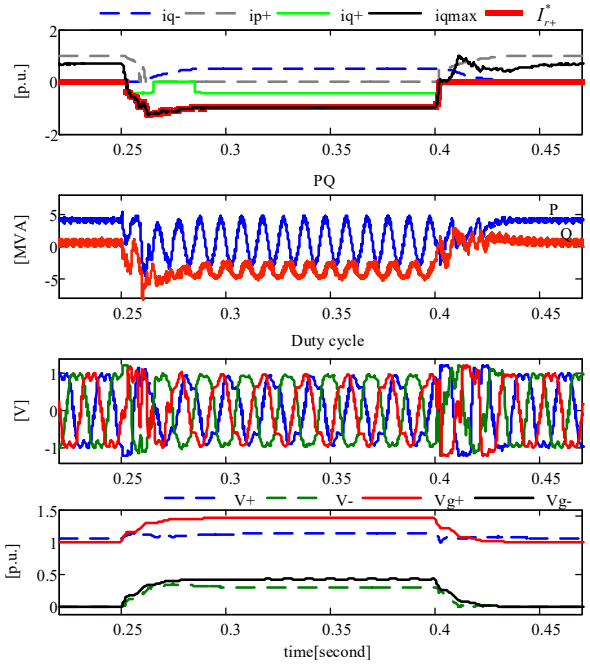

Figure 16. Voltage faults: V_{ag} = 0.5 p.u., V_{bg} = 1.8 p.u., V_{cg} = 1.8 p.u., with anti-saturation for SCR = 5. From top to bottom: in first figure active current reference, reactive current reference and the maximum available reactive current reference; in second figure active and reactive output power of converter; in third figure duty cycle; and in fourth figure magnitude of positive and negative sequence of PCC voltage and grid voltage.

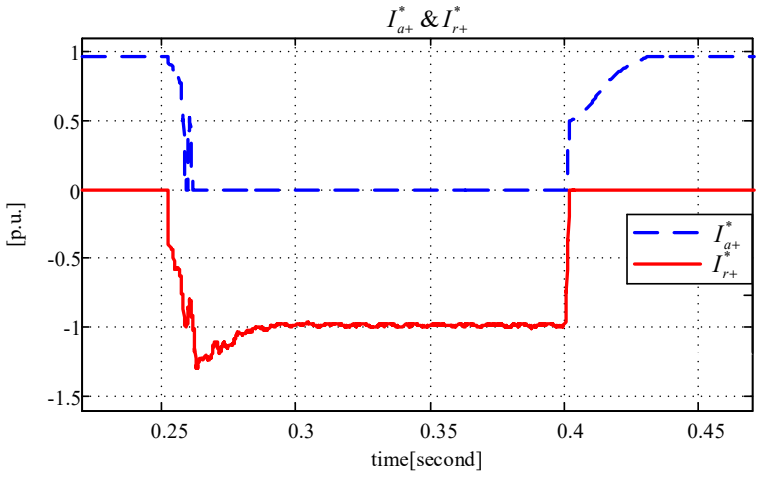

Figure 17. Set points of active and reactive currents in positive sequence for voltage faults: V_{ag} = 0.5 p.u., V_{bg} = 1.8 p.u., V_{cg} = 1.8 p.u., with anti-saturation for SCR = 5.

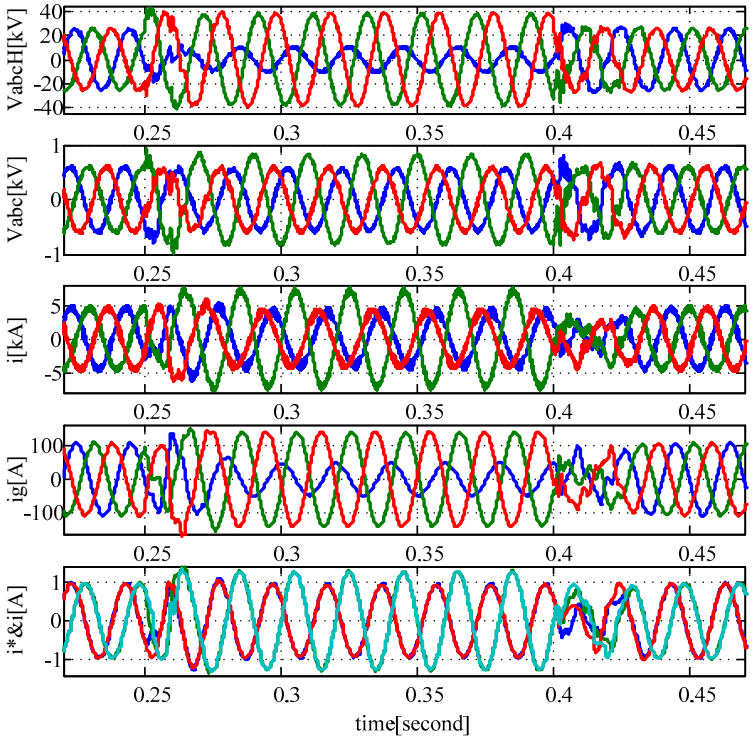

Figure 18. Voltage faults: V_{ag} = 0.5 p.u., V_{bg} = 1.8 p.u., V_{cg} = 1.8 p.u. From top to bottom: in first figure the voltage of grid; in second figure PCC voltage; in third figure converter current; and in fourth figure the current of grid and in fifth figure actual and reference currents in $\alpha\beta$ axes.

In the second scenario, a single-phase to ground unbalanced voltage sag for the grid with SCR = 2 is presented all while the negative sequence current is not injected to the PCC during voltage fault. The value negative sequence voltage for grid, PCC and inverter are the same due to the negative current is zero. The k_{v+} droop coefficient is set to 6 to show the performance of anti-saturation scheme. The obtained results are shown in Figures 19–21.

As it can be seen in the plots the V_{band} is 0.1 p.u. and the magnitude of positive sequence voltage is lower 0.9 and it has some fluctuations. Hence, $\Delta V_+ = 1 - |V_+|$ is higher than 0.1 and the inverter has to inject reactive current (reactive power) to PCC. Based on (3): $i_{q+} = K_{v+}(\Delta V_+ - 0.1)$. According to [28], k_{v+} droop coefficient has to be higher than 2. To show performance of proposed scheme in limiting reactive current set point (I^*_{r+}), k_{v+} is set 6.

From Figure 19, it can be seen that during the fault the value of the positive sequence reactive current reference i_{q+} is around 0.6 p.u., which leads to the controller saturation. Therefore, i_{q+} is cropped by the anti-saturation scheme to around 0.25 p.u. to prevent uncontrollability. Therefore, i_{q+} is around 0.6 p.u. and I^*_{r+} is around 0.25 p.u. The results in Figure 20 show the set points of positive sequence active and reactive currents. The active current is not limited because the converter current is lower than the nominal value.

The voltage and current waveforms of the grid and the PCC in the case of a single-phase unbalanced sag (type B—second scenario) are shown in Figure 21. In the high voltage side of transformer, only the voltage of phase A is reduced. Likewise, the voltage of the PCC is unbalanced and distorted similar to the high side of transformer. As it can be seen, in spite of the voltage at the PCC, the proposed outer loop generates correctly the reference currents. The PR controller later tracks this current reference without giving rise to any overshoot or steady state error, endorsing thus the good performance of the proposed control scheme. It is clear from the current waveforms that the peak value is below than the maximum nominal value. In addition, the grid and the converter currents have a satisfactory performance.

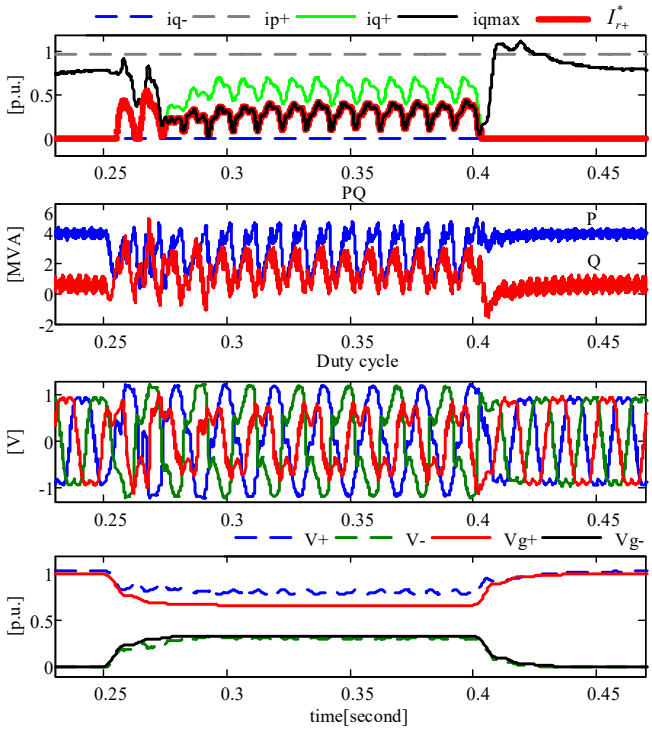

Figure 19. Voltage faults: 1ph 100% voltage sag without injecting negative sequence current with anti-saturation for SCR = 2. From top to bottom: in first figure active current reference, reactive current reference and the maximum available reactive current reference; in second figure active and reactive output power of converter; in third figure duty cycle; and in fourth figure magnitude of positive and negative sequence of PCC voltage and grid voltage.

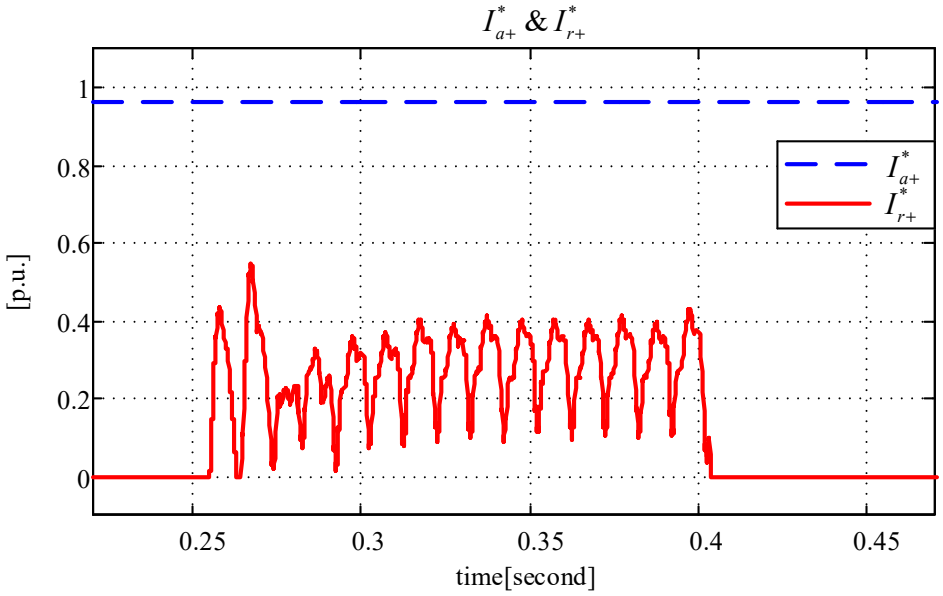

Figure 20. Set points of active and reactive currents in positive sequence in case of 1ph 100% voltage sag without injecting negative sequence current.

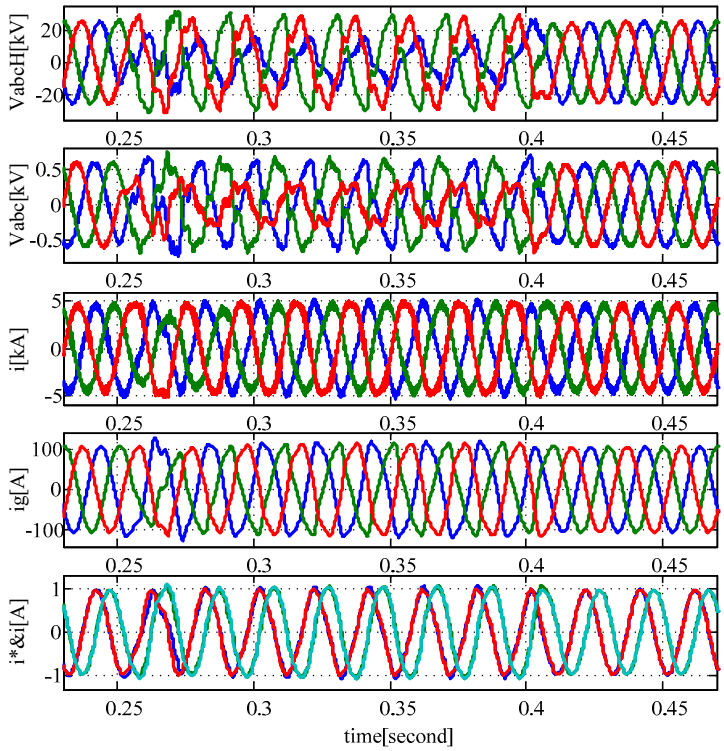

Figure 21. Voltage faults: 1ph 100% voltage sag without injecting negative sequence current. From top to bottom: in first figure the voltage of grid; in second figure PCC voltage; in third figure converter current; and in fourth figure the current of grid and in fifth figure actual and reference currents in $\alpha\beta$ axes.

4. Conclusions

In this paper, a proposal for overcoming the uncontrollability and instability issues of GC-VSC that appear under certain conditions linked to the fulfilment of LVRT requirement was presented. In this work, it was mathematically proven that GC-VSC may lose controllability under different operating conditions. For instance, under normal grid conditions when absorbing/injecting a high value of reactive power in capacitive/inductive mode or under severe grid fault scenarios due to the generation of unsuitable current/power references. In order to keep the GC-VSC under control, a new scheme with two parts were embedded to the outer reference generation loop and the inner current loop. A new PR controller with anti-windup capability was introduced as a controller in the current loop. Compared to other anti-windup implementations, the proposed solution has shown a good performance for integrating wind-up in PR controller, as well as to keep the output currents always limited and sinusoidal. Concerning the reference generation loop, the proposed reference modifier has shown that it is able to adjust the reactive reference taking into account the grid conditions and the operation points, with no need of knowing the grid voltage and impedance. The validation carried out in this work has permitted to demonstrate that the proposed scheme is a very suitable solution for accurately keeping the GC-VSC within its optimal operation boundaries under generic grid conditions.

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Author Contributions: Mahdi Shahparasti proposed the control scheme, conducted the analysis and validated the method. Pedro Catalán endorsed the performance of this scheme for the industrial high power converter and validated the results. Nurul Fazlin Roslan helped in the analysis part and the writing of the final version of the paper. Raúl-Santiago Muñoz-Aguilar contributed in the tunning of the current scheme parameters. Joan Rocabert

was in charge of the real time validation of the proposed system. Alvaro Luna proposed contributed to select the topic, determine the study case and he conducted the overall supervision of the paper.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

AC	Alternating Current
DC	Direct Current
C_f	capacitor of LC filter
IGBT	Insulated-Gate Bipolar Transistor
i_{abc}	current of the converter
$\mathrm{i}_{\mathrm{abcg}}$	current of the grid
$i^*_{\alpha+}$, $i^*_{\beta+}$	positive sequence components of converter current reference in stationary reference frame
$i^*_{\alpha-}$, $i^*_{\beta-}$	negative sequence components of converter current reference in stationary reference frame
i_{p+}, i_{q+}	active and reactive components of inverter current in positive sequence
i_{p-}, i_{q-}	active and reactive components of inverter current in negative sequence
I^*_{a+}, I^*_{r+}	set points of active and reactive current in positive sequence
I^*_{a-}, I^*_{r-}	set points of active and reactive current in negative sequence
I^*_{p+}, I^*_{q+}	active and reactive current command in positive sequence
f	fundamental frequency in Hz
FLL	frequency locked loop
k_f	feedforward gain
K_p	proportional gain
K_i	resonant gain
K_w	anti-windup gain
$k_{v\pm}$	droop coefficient
LC filter	Inductor-Capacitor filter
LPF	Low Pass Filter
KVL	Kirchhoff's Voltage Law
LVRT	Low Voltage Ride Through
L_f	inductor of LC filter
m	modulation index
m_{max}	maximum modulation index
O_α, O_β	output of PR controller with two integrators
O^*_α, O^*_β	output of PR controller after modification by anti-wind up or limiter
PCC	point of common coupling
*P**	active power reference
P	active power injected by the inverter to the PCC
PR	proportional-resonant
Q	reactive power injected by the inverter to the PCC
*Q**	reactive power reference
S	apparent power injected by the inverter to the PCC
SCR	short circuit ratio
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
t_{dead}	switching dead time
Ts	switching period
V_{dc}	DC bus voltage
V_{abc}	phase voltages of the PCC
V_{abcg}	phase voltages of the grid
V_{abci}	output voltage of inverter
V_i	space vector of output voltage of inverter
V_g	space vector of grid voltage

$V_{\alpha 1+}$, $V_{\beta 1+}$	fundamental components of positive sequence of PCC voltage in stationary reference frame
$V_{\alpha 1-}$, $V_{\beta 1-}$	fundamental components of negative sequence of PCC voltage in stationary reference frame
V_+, V_-	space vector of PCC voltage in positive and negative sequences
$V_{\alpha g1+}$, $V_{\beta g1+}$	fundamental components of positive sequence of grid voltage in stationary reference frame
$V_{\alpha g1-}$, $V_{\beta g1-}$	fundamental components of negative sequence of grid voltage in stationary reference frame
V_{g+}, V_{g-}	space vector of grid voltage in positive and negative sequences
Zg	equivalent grid impedance
$Z_f = X_f = 2\pi f L_f$	impedance of L_f
ω_o, ω_c	resonant frequency in rad/s and resonant bandwidth in rad/s

Subscripts and Superscripts

a,*b*,*c*	Phase
i	Inverter
g	Grid
max	Maximum
+,−	Positive sequence and negative sequence, respectively
*	Reference
–	complex conjugate

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