

Article

# Step-Up Partial Power DC-DC Converters for Two-Stage PV Systems with Interleaved Current Performance

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**Abstract:** This work presents a partial power converter allowing us to obtain, with a single DC-DC converter, the same feature as the classical interleaved operation of two converters. More precisely, the proposed topology performs similarly as the input-parallel output-series (IPOS) configuration reducing the current ripple at the input of the system and dividing the individual converters power rating, compared to a single converter. The proposed topology consists of a partial DC-DC converter processing only a fraction of the total power, thus allowing high efficiency. Experimental results are provided to validate the proposed converter topology with a Flyback-based 100 W test bench with a transformer turns ratio  $n_1 = n_2$ . Experimental results show high performances reducing the input current ripple around 30%, further increasing the conversion efficiency.

**Keywords:** DC-DC converters; microinverter; string inverter; partial power converters; photovoltaic energy

## 1. Introduction

Interleaved converters are widely used among power electronic applications. Such configurations can be adopted for different reasons in view of the features and benefits of the interleaved scheme. The two main advantages are:

- Distribution of the power among several converters, thus allowing us to reduce the power rating of the individual converters.
- Ripple reduction at the input and/or output of the converter when phase shifted carriers are used in the modulation, thus allowing reduction in the filters size.

Improvement in reliability is another among several advantages of interleaved configurations, making it possible to operate under failure of an individual converter thanks to the redundancy [1]. An additional advantage is the possibility of obtaining higher conversion ratio if input-parallel output-series (IPOS) or input-series output-parallel (ISOP) schemes are adopted. On the other hand, the main drawback is the increase in number of the power converters required in interleaved configurations.

In this work, a partial power DC-DC converter is proposed. It performs a step-up operation, and it is based on a Flyback topology with a transformer turns ratio  $n_1 = n_2$  in order to improve the input current performance. However, the turns ratio can vary when higher voltage gains are required but it could reduce the performance of the input current, leading into higher current ripples. Compared to a classical DC-DC converter, the proposed topology performs similarly to the IPOS configuration, reducing the current ripple at the input of the system and reducing the converter power

rating. The traditional IPOS interleaved converter scheme and main waveforms are given in Figure 1, for the case of Flyback topology. This specific topology has been used in several application such as two-stage photovoltaic (PV) inverters [2,3].

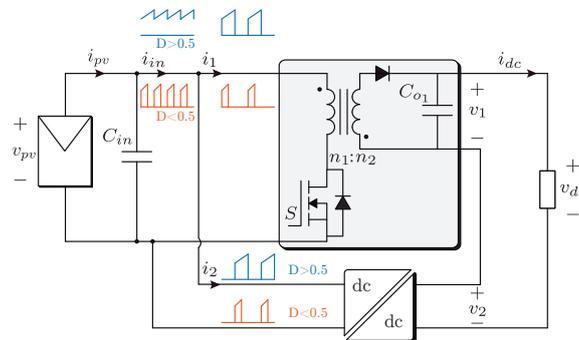


Figure 1. Traditional interleaved configuration using a Flyback topology.

## 2. Proposed Topology

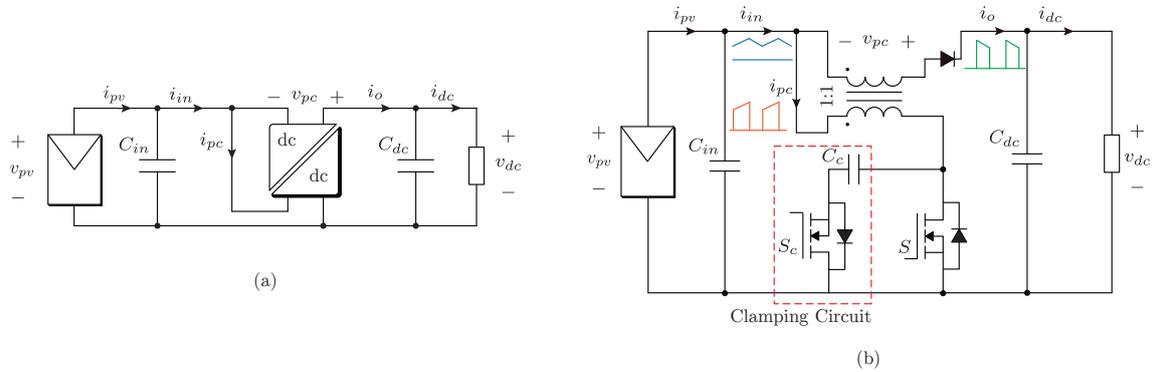
### 2.1. Partial Power Converters

The Partial Power Converter (PPC) concept has been around in other applications such as wind turbines, by using a doubly fed induction generator with an indirect four quadrant AC-DC-AC converter connected between the rotor windings [4] and the grid, and an additional direct grid connection to the stator. In this case the converter is only rated at 30% of the wind turbine power; yet it provides enough control range to perform variable speed operation and maximum power point tracking. The PPC concept oriented to PV systems was introduced in [5], in order to reduce the power losses inherent in two-stage configurations. The operation principle is based on the power biasing, establishing a series path between the input and output side. In essence the operating principle is to connect a series voltage between the PV system and the DC-link of the inverter. Since this voltage is usually smaller than the other two, it will process less power. It has been shown that the PPC concept improves the system efficiency compared to a classical full power converter. The PPC can also significantly reduce the converter size and power loss [6]. In this work the efficiency achieved working with a rated power lower than 30% is around 95%. For those reasons, the PPC concept has been used for various applications such as photovoltaic module integrated converter [7], PV powered electric aircraft [8], and distributed architectures. In those applications, the achieved efficiency is higher than 89% and 95% respectively, when the power processed is lower than 25% of the rated power. Other applications based on the same series connection are found in [9,10], where a 25 kW prototype was developed. The topology used for the experiment were four Full-bridge converters connected in series, designed to handle 30.7% of the rated power and achieving an efficiency around 96% working at 33 kHz. In [11–14], the focus is on the use of PPC for microinverter configurations. They present an improvement in the conversion efficiency, which is commonly a problem in microinverters due to the high voltage elevation required for the grid-connection. In those evaluation cases, the conversion efficiency is around 94% when the power processed by the converter is lower than 30% of the rated power. It concludes that the conversion efficiency increases by reducing the power processed by the converter.

### 2.2. Topology Description

The proposed partial power converter topology is depicted in Figure 2a. It consists of an isolated DC-DC converter connected following the PPC concept, so that the output  $v_{dc}$  of the system is the sum of the PV voltage  $v_{pv}$  and the converter output  $v_{pc}$ . It should be noticed that even if the converter used has a HF transformer, due to the PPC connection the resulting conversion PV system does not

provide galvanic isolation. This might be seen as a drawback, but considering that the power rating of the converter will be much lower than the total power, this is not a significant issue. Furthermore, the grounding of the PV system can be achieved by proper selection of the inverter stage and modulation, as with traditional transformer-less PV inverters [15].



**Figure 2.** (a) Configuration of the partial power converter. (b) Proposed topology using a Flyback converter.

In Figure 2b, the proposed converter is represented as a Flyback converter with clamping circuit such as it has been validated in Experimental section. In Figure 2b the current typical waveforms are also shown.

In general terms, no matter the PPC configuration nor the isolated DC-DC topology, the voltage gain  $G_v$  of the DC-stage is expressed as:

$$G_v = \frac{V_{dc}}{V_{pv}} \tag{1}$$

Moreover, considering that the input and output capacitors losses are neglected, the DC-stage conversion efficiency  $\eta_{dc_s}$  is expressed as:

$$\eta_{dc_s} = \frac{V_{dc} I_o}{V_{pv} I_{in}} \tag{2}$$

Including (1) in (2), then the efficiency is expressed as:

$$\eta_{dc_s} = G_v \frac{I_o}{I_{in}} \tag{3}$$

By Kirchoff laws, the voltage and current shown in Figure 2a are expressed as:

$$V_{dc} = V_{pv} + V_{pc} \tag{4}$$

$$I_{in} = I_{pc} + I_o \tag{5}$$

In general terms, the partial power ratio  $K_{pr}$  is defined as:

$$K_{pr} = \frac{P_{pc}}{P_{pv}} \tag{6}$$

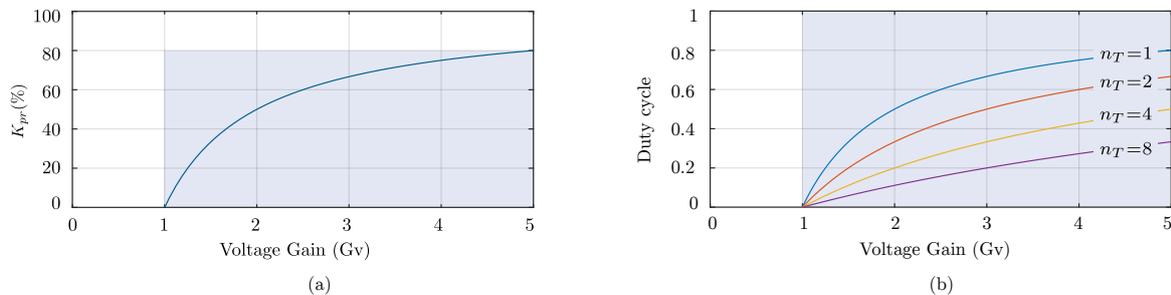
And, in order to define the operation region of the Step-Up PPC, the partial power ratio  $K_{pr}$  is calculated as:

$$\begin{aligned}
 K_{pr} &= \frac{V_{pv} I_{pc}}{V_{pv} I_{in}} \\
 K_{pr} &= \frac{I_{in} - I_o}{I_{in}} \\
 K_{pr} &= 1 - \frac{I_o}{I_{in}}
 \end{aligned}
 \tag{7}$$

In order to express the  $K_{pr}$  in terms of the DC-stage efficiency and voltage gain, (3) is included in (7) and the partial power ratio is finally defined as:

$$K_{pr} = 1 - \frac{\eta_{dc_s}}{G_v}
 \tag{8}$$

Considering that the DC-stage is highly efficiency  $\eta_{dc_s} \approx 1$ , the partial power ratio  $K_{pr}$  varies depending on the voltage gain  $G_v$  as depicted in the Figure 3a. Where the shadowed area represents the region of partial power operation.



**Figure 3.** (a) Partial power operation range of the Step-Up Partial Power Converter (PPC). (b) Operation range of the Step-Up Flyback based PPC for different transformer turns ratio  $n_T$ .

### Analysis of Topology

Commercial DC-DC converters for PV applications are based on traditional topologies. Among the criteria for the topology selection are the complexity of the structure, the control technique, reliability and efficiency [15]. The operation of the PPC in terms of duty cycle varies depending on the isolated DC-DC topology. In this section the traditional Flyback converter is chosen not only because its simple structure and high applicability in the PV industry [16,17]. But also because its operation features as will be analyzed in this section. Nevertheless, the same analysis can be made for different isolated DC-DC topologies.

This analysis is based on the operation range, which means that the converter must have the ability to elevate the voltage and work as a PPC within the duty cycle range  $d = [0-1]$ . Moreover, is also analyzed the importance and dependence of the transformer turns ratio  $n_T$  in the operation range.

Working with a Flyback topology for the PPC configuration, and connecting as depicted in Figure 2b, the DC-DC converter voltage gain  $G_{vc}$  is calculated as:

$$G_{vc} = \frac{V_{pc}}{V_{pv}} = \frac{n_T d}{1 - d}
 \tag{9}$$

Applying (4), the equation can be expressed as:

$$\frac{V_{dc} - V_{pv}}{V_{pv}} = \frac{n_T d}{1 - d}
 \tag{10}$$

Rearranging and simplifying the expression, also considering that  $G_v = V_{dc}/V_{pv}$ . Then the global voltage gain can be expressed as:

$$G_v = \frac{1 + d(n_T - 1)}{1 - d} \quad (11)$$

The voltage gain (11) depends on the duty cycle  $d$ , which is limited to  $[0-1]$ , and the transformer turns ratio  $n_T$ . The operation range is depicted in Figure 3b, where the shadowed area represents the region of partial power operation.

From this picture it is possible to see that using a Flyback topology for the PPC configuration, the converter operation is not limited by the voltage gain, but the transformer turns ratio. For example, considering a small voltage gain (e.g,  $G_v < 2$ ), and a turns ratio  $n_T = 8$ , the duty cycle range is limited to  $d = [0-0.11]$ . It means that a high resolution in the control platform is needed to compensate the small variations, which is translated to a more expensive control design. Instead, with a transformer turns ratio  $n_T = 1$ , the duty cycle range increases to  $d = [0-0.5]$  for the same application. The same analysis can be applied for higher voltage gains, where the best resolution is achieved by using a transformer with greater turns ratio.

At this point it is worth enhancing the advantages of the presented topology. The waveforms in Figure 2b show one of the advantages respect to the traditional IPOS configuration. Indeed, the input current of the proposed topology  $i_{in}$  is the sum of the current  $i_{pc}$  and  $i_o$ . As those currents are complementary, the resulting current  $i_{in}$  will be continuous for any duty cycle if the converter operates under continuous conduction mode (CCM). Moreover, with the transformer turn ratio  $n_1/n_2 = 1$  both, the current  $i_{pc}$  and  $i_o$  have the same peak value, which leads in a continuous input current  $i_{in}$ . On the other side, in the case of the traditional IPOS configuration realized with Flyback converters, the input current  $i_{in}$  shown in Figure 1 is discontinuous for duty cycles lower than 0.5.

### 3. Experimental Results

The experimental test bench shown in Figure 4 was built to validate the operation of the proposed topology. The PV system is emulated with the programmable DC-power supply Chroma 62050H-600S, with Solar Array Simulator (600 V/5 kW). The control platform is composed of a dSPACE 1103 controlling the DC-DC converters, a FPGA Spartan-3E generating the high-frequency PWM signals, and an interface board between the dSPACE and the FPGA. The PPC are used to perform the Maximum Power Point Tracking (MPPT) algorithm controlling the input voltage, and the output voltage is fixed by the DC-power supply Agilent N8762A Technologies (600 V/8.5 A) to emulate the grid-tied inverter. The power delivered by the PV system is dissipated in a resistive load.

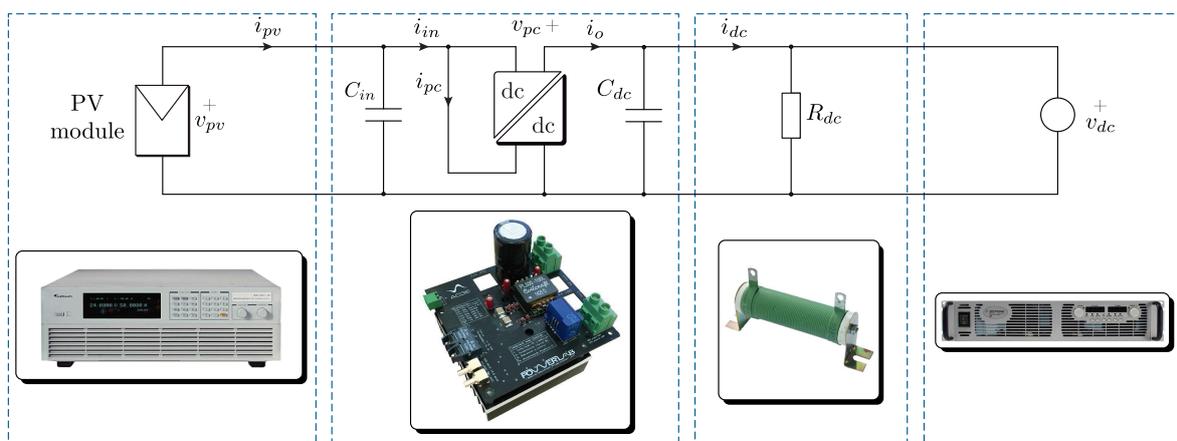


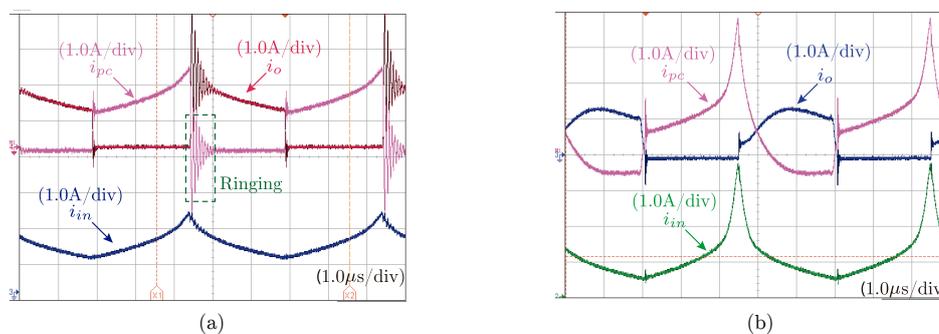
Figure 4. Experimental test bench for the evaluation of the proposed converter.

For the prototype construction, a HF transformer (Coilcraft PL300-100L) is included, which has the transformer turns ratio  $n_1:n_2 = 4:4$  and it is rated to  $P = 300$  W. The Mosfet (IRFB4019PBF) rated to 17 A@150 V and the Diode (12TQ150(S)) rated to 15A@150 V.

The parameters of the Step-Up Flyback based PPC are: PV voltage  $v_{pv} = 30$  V, input capacitance  $C_{in} = 10$   $\mu$ F, clamping capacitance  $C_c = 5$   $\mu$ F, output capacitance  $C_{dc} = 1000$   $\mu$ F, transformer turns ratio  $n_1:n_2 = 4:4$  and switching frequency  $f_{sw} = 200$  kHz.

### 3.1. Clamping Circuit

Firstly, the proposed Flyback-based partial power converter was tested without clamping circuit. Measured currents are shown in Figure 5 for the converter working with a duty cycle  $D = 0.48$ . In this figure, it can be seen that the resulting input current  $i_{in}$  behave as expected and represented in Figure 2b, being a continuous waveform with reduced ripple around 50% compared with a traditional Flyback converter. In Figure 5a, it can also be observed the presence of an important ringing effect when the main switch turns off. This ringing effect is due to the presence of parasitic elements in the circuit, combined with the fast switching of the devices working at the frequency  $f_{sw} = 200$  kHz. Such phenomenon is not desirable since it implies high stress in the devices resulting in higher losses.

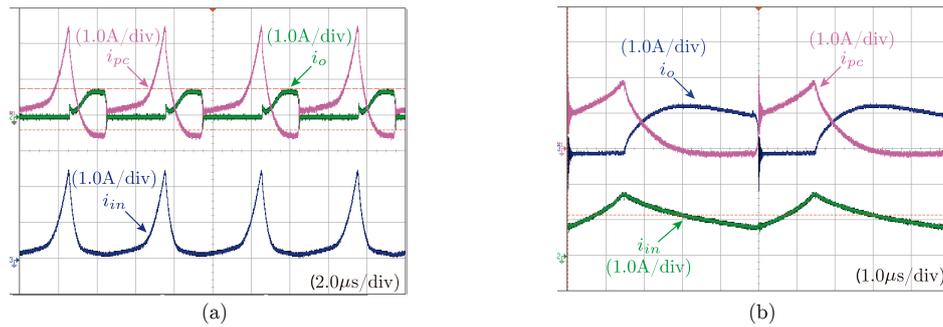


**Figure 5.** Current measurements in the proposed converter. (a) Without the clamping circuit and  $D = 0.48$ . (b) With the clamping circuit and  $D = 0.48$ .

In order to mitigate the ringing effect, a clamping circuit as represented in Figure 2b is used. Measured currents are shown in Figure 5 (b) for the converter working with the same duty cycle  $D = 0.48$ , this time using the clamping circuit. As a result of the addition of the clamping circuit, it can be observed that the undesired ringing effect is no more present. The current waveforms are little modified, because of the clamping capacitor  $C_c$  included in the auxiliary circuit. However, the main behavior of the converter is similar, in particular regarding the input current  $i_{in}$  being continuous and with reduced ripple around 30% compared with a traditional Flyback converter.

### 3.2. Converter Operation with $D = 0.63$

Additional tests have been done to validate the operation of the proposed partial power converter topology under different operating points. First, results are proposed operating the converter with  $D = 0.63$ . Figure 6a gives the measured currents. Once again it can be observed that the resulting input current  $i_{in}$  is continuous as observed.



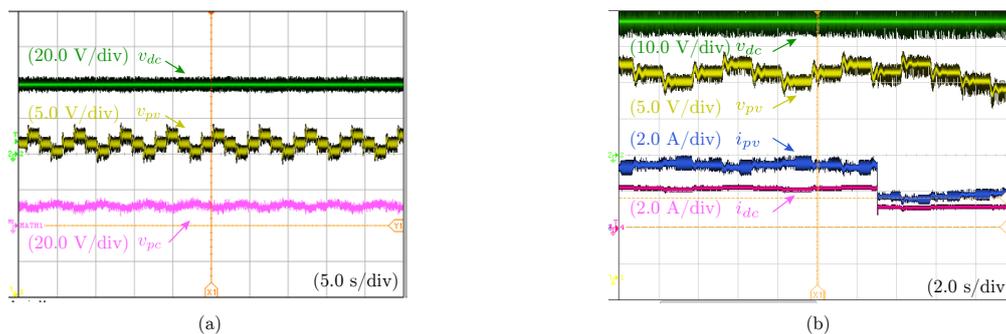
**Figure 6.** Current measurements. (a) With the clamping circuit and  $D = 0.63$ . (b) With the clamping circuit and  $D = 0.28$ .

### 3.3. Converter Operation with $D = 0.28$

The behavior of the proposed topology has also been verified for duty cycles lower than 0.5. Figure 6b gives the currents of the converter operating with  $D = 0.28$ . As described in Section 2.2, the proposed topology shows one of its major advantage in contrast to the traditional IPOS configuration while the converter operates with a duty cycle lower than 0.5. Indeed, in Figure 6b, it is verified that for a low duty cycle operation, the input current  $i_{in}$  is continuous. On the other hand, in the case of the traditional IPOS configuration made with Flyback converters, the input current  $i_{in}$  as represented in Figure 1 is discontinuous for duty cycle lower than 0.5.

Under constant solar irradiation the parameters evaluated are the voltage and current in the system. The voltages are depicted in Figure 7a, where the P&O MPPT algorithm presents the classical three levels. In traditional PV applications the voltage at the DC-link  $v_{dc}$  is fixed by the inverter, then due to the series connection of the PPC, the converter voltage  $v_{pc}$  is the difference between  $v_{dc}$  and  $v_{pv}$ .

The experimental results of the MPPT performance are depicted in Figure 7b, where an irradiation change is made reducing the value around  $\approx 50\%$ . In this proposed work the Perturb & Observe (P&O) algorithm is implemented due to the simple implementation and effective tracking of the MPP [18]. It is possible to note the constant output voltage  $v_{dc}$ , the current reduction at the input  $i_{pv}$  and output side of the converter  $i_{dc}$  depending on the irradiation change. Moreover, the PV voltage  $v_{pv}$  varies until find the maximum power point, where the typical three levels are depicted oscillating around the MPP.



**Figure 7.** Maximum Power Point Tracking (MPPT) performance in the Step-Up based PPC: (a) under constant solar irradiation; (b) under a solar irradiation change.

### 3.4. Converter Efficiency

In order to obtain the experimental efficiency, the power is calculated using the modulated and sampled values of voltage and current. The measurements are taken from the whole power conversion

system (PPC configuration), and the isolated DC-DC converter used to make the configuration (Flyback topology).

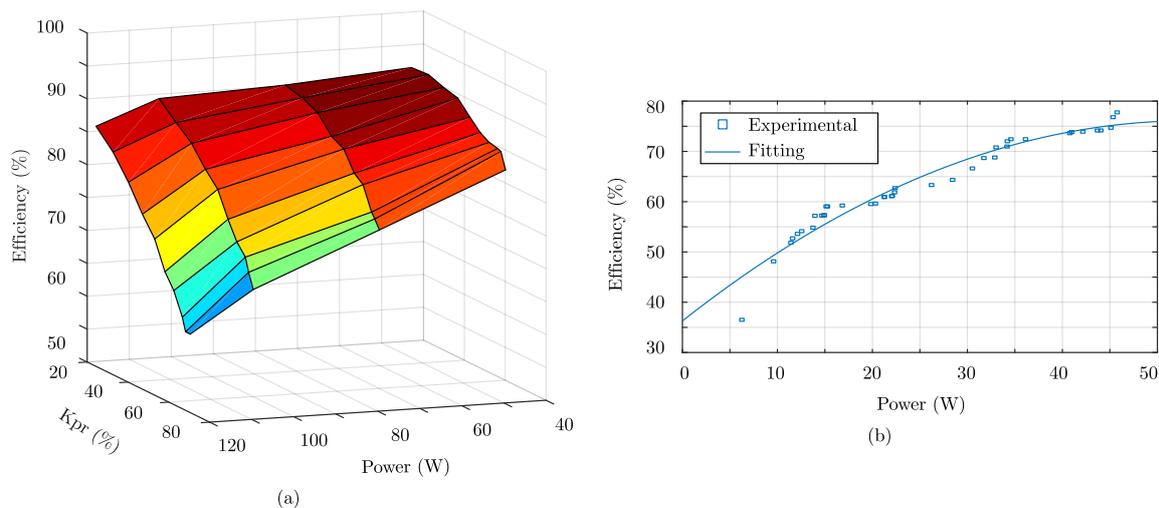
The DC-stage efficiency  $\eta_{dc_s}$ , which represents the global conversion efficiency, is calculated based on the measurements at the output side ( $I_o, V_{dc}$ ) and the input side ( $I_{pv}, V_{pv}$ ).

$$\eta_{dc_s} = \frac{V_{dc} I_o}{V_{pv} I_{pv}} \quad (12)$$

On the other hand, the DC-DC efficiency  $\eta_{dc_c}$  represents the conversion efficiency of the isolated Flyback DC-DC converter used for making the PPC configuration. It is calculated based on the measurements at the output side of the DC-DC Flyback converter ( $I_o, V_{pc}$ ) and the input side ( $I_{pc}, V_{pv}$ ).

$$\eta_{dc_c} = \frac{V_{pc} I_o}{V_{pv} I_{pc}} \quad (13)$$

The experimental efficiency waveforms are depicted in Figure 8. The global conversion efficiency of the DC-stage is obtained under different power and partial power ratios  $K_{pr}$ . When the converter is operating below  $K_{pr} \leq 80\%$  of the total power, the global conversion efficiency varies between 70–90%, as depicted in Figure 8a. On the other hand, the conversion efficiency of the DC-DC converter varies between 35–77%, as depicted in Figure 8b, where it is also possible to note the experimental points obtained from measurements and the curve fitting. This can be understood in the sense that the Flyback converter is handling a very low power, in comparison for which it was designed. Moreover, the topology operates with a deep voltage gain as will be explained.



**Figure 8.** Curve of experimental efficiency: (a) Total power conversion system. (b) Isolated DC-DC converter in the Step-Up Flyback based PPC.

In order to enhance the analysis of efficiency, Table 1 illustrates an experimental operating point for the configuration. As can be seen, the PV system is rated at  $P_{pv} = 99$  W but it is handling a  $K_{pr} = 20\%$  of the total power. The partial power ratio  $K_{pr}$  is related to the global voltage gain, which is  $G_v = 1.17$ . However, due to the series connection, the voltage at converter side is very small  $V_{pc} = 4.8$  V, which leads to a deep voltage gain for the isolated Flyback DC-DC converter  $G_{vc} = 0.15$ . That is the reason because of the low efficiencies reached with the Flyback converter. However, from the point of view of the whole system it is not a problem when the partial ratio is low, because the DC-DC converter is handling a low power. Therefore, the power loss related to the DC-DC conversion is  $P_{dc_l} = 8.12$  W, which represents the 8.2% of the global system losses.

**Table 1.** Experimental evaluation points.

Parameters	Value	Parameters	Value
System Power (W)	99	Converter voltage (V)	4.8
DC-DC Power (W)	19.8	Global Voltage gain $G_v$	1.17
$K_{pr}$ (%)	20	DC-DC Voltage gain $G_{vc}$	0.15
Input voltage (V)	27.9	DC-stage efficiency $\eta_{dc_s}$ (%)	90
Output voltage (V)	32.7	DC-DC efficiency $\eta_{dc_c}$ (%)	59

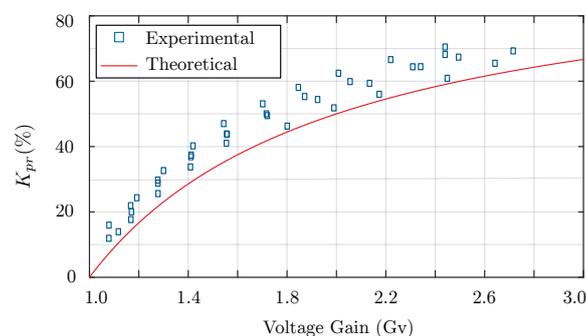
Moreover, as can be realized the DC-DC converter works as buck converter despite of the step-up operation. It means that the topology operation does not define the operation of the PPC configuration. For that reason, for this application it is important to select a topology with a buck-boost operation in order to compensate the required converter voltage  $v_{pc}$ . That is also a motivation to use a Flyback instead of other topologies, so that with a turns ratio  $n_1 = n_2$  the voltage gain is not limited because of the inherent buck-boost operation.

Laboratory prototypes are not optimized in their design in terms of efficiency for the power rating in which they operate, particularly due to the fact that semiconductors and modules are designed for full power operation. Consequently, it is expected that for commercial developments, which are optimized in terms of efficiency for a particular power rating, improved efficiencies can be obtained for the DC-DC converter stages, further improving the global system efficiency. In addition, the main point of the contribution is to highlight the increment of the efficiency achieved with the PPC configuration, despite of the lower efficiency of the Flyback DC-DC converter used for the the construction of the PPC.

#### 4. Analysis of the Partial Power Ratio

In order to evaluate the ratio of power processed by the converter, the voltage and current are measured at the Mosfet bridge, and the mean value is multiplied in order to obtain the converter power  $P_{pc}$ . Then, it is divided by the input power  $P_{pv}$  in order to obtain the partial power ratio  $K_{pr}$ . The experimental results are shown with points and the theoretical value is shown with a continuous line.

The experimental result for the Step-Up Flyback based PPC is depicted in Figure 9. It is possible to notice the increase of  $K_{pr}$  when the voltage gain is also increasing. The behavior fits with the theoretical result in (8). Nevertheless, it presents a small bias but it can be explained in the sense that the theoretical analysis was made considering a global efficiency  $\eta_{dc_s} = 1$ . Nevertheless, the important fact is the validation of the dependence between the voltage gain and the power processed by the converter.

**Figure 9.** Experimental partial power ratio for the Step-Up Flyback based PPC.

#### 5. Conclusions

In this work, a partial power converter with interleaved current performance has been proposed. The main feature of the converter consists to obtain, with a single PPC, the current improvement obtained in a classical IPOS configuration of two converters. The proposed topology has been validated

in a Flyback-based 100 W laboratory prototype. The experimental results validated the operation depicting a continuous current at the input of the converter, and current ripple reduction around 30%. It is useful in PV applications because it allows a size reduction of the input capacitor filter. In addition, the MPPT performance was also validated under an irradiation change, by using the P&O algorithm. Finally, the tested experimental prototype reaches higher conversion efficiencies compared with the isolated DC-DC converter used to make the PPC configuration.

Future works will related to the evaluation of the IPOS configuration, working with interleaved PPCs. In order to increase the voltage gain, it is necessary to reduce the power processed by the converters even further, and to reduce the input current ripple.

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**Author Contributions:** Jaime Wladimir Zapata conceived, designed and performed the experimental evaluations. Gonzalo Carrasco was part of the team to develop the experimental test-bench. Samir Kouro and Hugues Renaudineau were responsible for the guidance and a number of key suggestions.

**Conflicts of Interest:** The authors declare there is no conflict of interest.

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