A Novel Step-Up Converter with an Ultrahigh Voltage Conversion Ratio

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Abstract: A new step-up converter with an ultrahigh voltage conversion ratio is proposed in this paper. Two power switches of such a converter, which conduct synchronically, and its output voltage, which has common ground and common polarity with its input voltage, lead to the simple control circuit. No abrupt changes in the capacitor voltage and the inductor current of the proposed step-up converter mean that it does not suffer from infinite capacitor current and inductor voltage. Two input inductors with different values can still allow the proposed step-up converter to work appropriately. An averaged model of the proposed step-up converter was built and one could see that it was still fourth-order even with its five storage elements. Some theoretical derivations, theoretical analysis, Saber simulations, and circuit experiments are provided to validate the effectiveness of the proposed step-up converter.

Keywords: new step-up converter; ultrahigh voltage conversion ratio; small-signal model; average-current mode control

1. Introduction

As part of a DC switching power supply, the step-up converter is important for transforming low input voltage into the desired high output voltage to satisfy the requirements of practical applications, such as photovoltaic (PV) systems, fuel-cell systems, etc. Step-up converters can be classified into two types: non-isolated and isolated. An isolated step-up converter is generally constructed by inserting a transformer into a non-isolated step-up converter to enlarge the voltage conversion ratio. However, switch voltage overshoot and EMI problems caused by the transformer make the whole system suffer from low efficiency and huge volume [1,2]. Therefore, the non-isolated step-up converter is the focus of many researchers and engineers. It is well known that the traditional boost converter with a voltage conversion ratio of $1/(1 - D)$, where D is the duty cycle, is a good topology to realize the boost ability because it has a simple structure [3]. Nevertheless, under certain input voltages, if an extremely high output voltage is required, the duty cycle must be close to 1.0, and this cannot generally be achieved because of the limitations of real semiconductors. Accordingly, in the last few decades, many researchers and engineers have made much effort to explore a novel step-up converter with a high voltage conversion ratio, and many effective topologies have been proposed. For example, for realizing a voltage conversion ratio of $(1 + D)/(1 - D)$, which is higher than that of the traditional boost converter, Yang et al. constructed a transformerless step-up converter [4], Gules et al. introduced a modified single-ended primary-inductor converter (Sepic) [5], and Mummadi proposed a fifth-order boost converter [6]. However, that voltage conversion ratio was limited to some extent.

To achieve a voltage conversion ratio which is higher than $(1 + D)/(1 - D)$ within a certain area of D, several step-up converters have been proposed. For example, for obtaining a voltage conversion ratio of $(2 - D)/(1 - D)$, the following converters have been proposed: KY boost converter constructed by combining a KY converter with a traditional synchronously rectified boost converter [7], a step-up converter constructed by combining KY and buck-boost converters [8], and an elementary positive output super-lift Luo converter [9]. For obtaining a voltage conversion ratio of $2/(1 - D)$, Hwu et al. combined the charge pump concept with the traditional boost converter to construct a fourth-order step-up converter [10], and Al-Saffar et al. integrated the traditional boost converter with a self-lift Sepic converter to introduce a sixth-order step-up converter [11]. Also, Hwu et al. proposed two voltage-boosting converters with a voltage conversion ratios of $(3 - D)/(1 - D)$ and $(3 + D)/(1 - D)$ by using bootstrap capacitors and boost inductors [12]. Chen et al. proposed an interleaved step-up converter with the voltage conversion ratio being $3/(1 - D)$ [13]. However, all of the above step-up converters possess an abrupt change in voltage across the capacitor, which limits them in practical applications to some extent. Moreover, like a boost converter, if an ultrahigh output voltage from those converters is required, the duty cycle D must be close to 1.0, and this also cannot generally be achieved because of the limitations of real semiconductors.

Therefore, for acquiring a higher output voltage with the same polarity as the input voltage with the duty cycle D being close to 0.5, which is very easy to implement in practical situations, some new DC-DC converters have been proposed. For example, in [14], based on a Sheppard- Taylor converter whose voltage conversion ratio of $-D/(1 - 2D)$ is negative, a modified Sheppard-Taylor converter with a voltage conversion ratio of $D/((1 - D)(1 - 2D))$ was proposed. Also, by removing some components of the Sheppard-Taylor converter, a simple modified Sheppard-Taylor converter with a voltage conversion ratio of $1/(1 - 2D)$ was proposed in [15]. However, its voltage conversion ratio of $1/(1 - 2D)$ was obtained under the unreasonable assumption that the voltages across its two capacitors were equal. In fact, its voltage conversion ratio was related to not only the duty cycle D, but also the load resistor and the switch frequency, so its load regulation is not good enough [16]. In addition, a fourth-order step-up converter with a voltage conversion ratio of $(1 - D)/(1 - 2D)$ was presented in [17] and a pulse-width modulation (PWM) Z-source DC-DC converter with the same voltage conversion ratio was investigated in [18]. However, their voltage conversion ratios were also limited to some extent. In particular, the output voltage of the PWM Z-source DC-DC converter was floating. Hence, exploring new step-up converters with good performance is very important and valuable. In this study, a new step-up converter with an ultrahigh voltage conversion ratio is proposed. In this converter, the output voltage is common-grounded with the input voltage, and its two power switches conduct synchronically. Even if the two input inductors have different values, the proposed step-up converter can still work appropriately. Additionally, there is no abruptly changing on the current through the inductors and the voltage across the capacitors.

This paper is organized as follows. In Section 2, the structure and basic principle of the proposed step-up converter in continuous conduction mode (CCM) is presented in detail. In Section 3, the averaged model and corresponding small-signal model are established and analyzed. Comparisons among existing step-up converters and the proposed step-up converter are presented in Section 4. Some Saber simulations and circuit experiments for confirmation are presented in Section 5. Finally, some concluding remarks and comments are given in Section 6.

2. Novel Topology's Structure and Its Basic Principle

A circuit schematic of the proposed step-up converter is shown in Figure 1. It consists of two power switches (Q_1 and Q_2), five diodes (D_1, D_2, D_3, D_4, and D_5), three inductors (L_1, L_2, and L_3), two capacitors (C_1 and C_2), and the resistive load R. Two power switches conduct synchronically and are driven by the same PWM signal v_d, with the period being T and duty cycle being d. The currents through the three inductors are denoted by i_{L1}, i_{L2} and i_{L3}. The voltages across the two capacitors are defined as v_{C1} and v_0. Notably, the proposed step-up converter operating in the continuous conduction

mode (CCM) is the only concern here, and its possible stages are shown in Figure 2. Based on the relation between inductors L_1 and L_2, there are three cases for the proposed step-up converter, case 1: $L_1 = L_2$, case 2: $L_1 < L_2$ and case 3: $L_1 > L_2$. The principle of the proposed step-up converter under the three cases is discussed in detail in the following subsections.
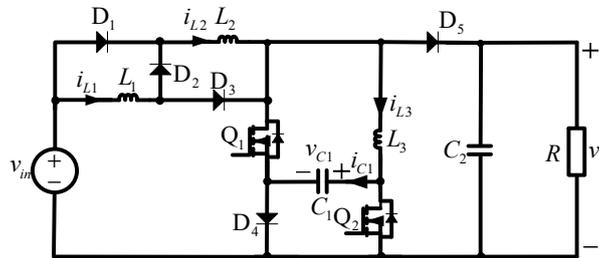

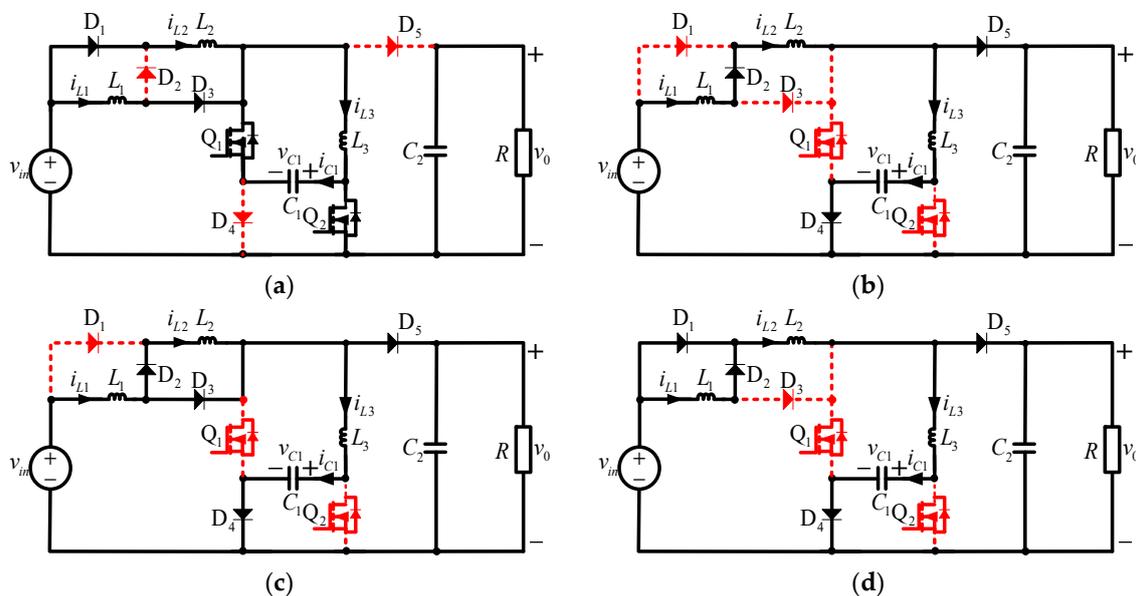**Figure 1.** Circuit schematic of the proposed step-up converter.

Figure 2. Equivalent circuits for possible stages of the proposed step-up converter in CCM. (**a**) Stage 1; (**b**) Stage 2; (**c**) Stage 3; (**d**) Stage 4.

2.1. Case 1: $L_1 = L_2$

For this case, the proposed step-up converter has only two operation stages; their equivalent circuits are shown in Figure 2a,b.

2.1.1. Stage 1

Figure 2a shows that two power switches (Q_1 and Q_2) are turned on for the high level of PWM signal v_d, and three of the diodes D_2, D_4 and D_5 do not conduct for the inverse biased voltage, whereas two of the diodes (D_1 and D_3) conduct for the forward biased voltage. That is, the state of power switches and diodes is: (Q_1, Q_2, D_1, D_2, D_3, D_4, $D_5 \equiv$ON, ON, ON, OFF, ON, OFF, OFF) within $NT < t \leq NT + dT$ where N is a natural number. Accordingly, the input voltage source supplies the energy to two input inductors (L_1 and L_2) so that both of them are magnetized and their currents increase. Because $L_1 = L_2$, the currents through these two inductors are equal, that is, $i_{L1} = i_{L2}$. Capacitor C_1 is in parallel with inductor L_3. Consequently, capacitor C_1 is discharged so that its voltage decreases

and inductor L_3 is demagnetized so that its current also decreases. In addition, capacitor C_2 delivers energy to the resistive load R. The associated equations for stage 1 are:

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{v_{in}+v_{C1}}{L_1} \\ \frac{di_{L2}}{dt} = \frac{v_{in}+v_{C1}}{L_2} \\ \frac{di_{L3}}{dt} = -\frac{v_{C1}}{L_3} \\ \frac{dv_{C1}}{dt} = \frac{i_{L3}-i_{L1}-i_{L2}}{C_1} \\ \frac{dv_0}{dt} = -\frac{v_0}{RC_2} \end{cases} \tag{1}$$

2.1.2. Stage 2

Figure 2b shows that two power switches (Q_1 and Q_2) are turned off for the low level of PWM signal v_d. Three diodes (D_2, D_4, and D_5) conduct, and the remaining diodes (D_1 and D_3) do not conduct. That is, the state of power switches and diodes is: (Q_1, Q_2, D_1, D_2, D_3, D_4, $D_5 \equiv$ OFF, OFF, OFF, ON, OFF, ON, ON) within $NT + dT < t \leq NT + T$. Hence, inductor L_1 is in series with inductor L_2, leading to $i_{L1} = i_{L2}$, and together with the input voltage v_{in}, they supply the energy to inductor L_3 and capacitor C_1. The corresponding equations for stage 2 are:

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{v_{in}-v_0}{L_1+L_2} \\ \frac{di_{L2}}{dt} = \frac{v_{in}-v_0}{L_1+L_2} \\ \frac{di_{L3}}{dt} = \frac{v_0-v_{C1}}{L_3} \\ \frac{dv_{C1}}{dt} = \frac{i_{L3}}{C_1} \\ \frac{dv_0}{dt} = \frac{i_{L1}}{C_2} - \frac{i_{L3}}{C_2} - \frac{v_0}{RC_2} \end{cases} \tag{2}$$

2.2. Case 2: $L_1 < L_2$

For case 2, besides stage 1 and stage 2, it has stage 3, as shown in Figure 2c, corresponding to (Q_1, Q_2, D_1, D_2, D_3, D_4, $D_5 \equiv$ OFF, OFF, OFF, ON, ON, ON, ON) within $NT + dT < t \leq NT + dT + d_{11}T$ because diode D_3 is still conducting for $i_{L1} > i_{L2}$. Its mathematical model is:

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{v_{in}-v_0}{L_1} \\ \frac{di_{L2}}{dt} = 0 \\ \frac{di_{L3}}{dt} = \frac{v_0-v_{C1}}{L_3} \\ \frac{dv_{C1}}{dt} = \frac{i_{L3}}{C_1} \\ \frac{dv_0}{dt} = \frac{i_{L1}}{C_2} - \frac{i_{L3}}{C_2} - \frac{v_0}{RC_2} \end{cases} \tag{3}$$

Notably, stage 3 will last until $i_{L1} = i_{L2}$, leading to the diode D_3 being off and the proposed step-up converter immediately operating in stage 2. Therefore, the sequence of operations of the proposed step-up converter in case 2 is: stage 1 (Figure 2a) during $NT < t \leq NT + dT$, stage 3 (Figure 2c) during $NT + dT < t \leq NT + dT + d_{11}T$, and stage 2 (Figure 2b) during $NT + dT + d_{11}T < t \leq NT + T$.

2.3. Case 3: $L_1 > L_2$

For case 3, besides stage 1 and stage 2, it has stage 4, as shown in Figure 2d, corresponding to (Q_1, Q_2, D_1, D_2, D_3, D_4, $D_5 \equiv$ OFF, OFF, ON, ON, OFF, ON, ON) during $NT + dT < t \leq NT + dT + d_{22}T$ because diode D_1 is still conducting for $i_{L1} < i_{L2}$. Its equations are:

$$
\begin{cases}
\frac{di_{L1}}{dt} = 0 \\
\frac{di_{L2}}{dt} = \frac{v_{in} - v_0}{L_2} \\
\frac{di_{L3}}{dt} = \frac{v_0 - v_{C1}}{L_3} \\
\frac{dv_{C1}}{dt} = \frac{i_{L3}}{C_1} \\
\frac{dv_0}{dt} = \frac{i_{L2}}{C_2} - \frac{i_{L3}}{C_2} - \frac{v_0}{RC_2}
\end{cases}
\tag{4}
$$

Please note that stage 4 will end if $i_{L1} = i_{L2}$, which prevents diode D_1 from conducting and the proposed step-up converter will immediately operate in stage 2. Therefore, the sequence of operations of the proposed step-up converter in case 3 is: stage 1 (Figure 2a) during $NT < t \le NT + dT$, stage 4 (Figure 2d) during $NT + dT < t \le NT + dT + d_{22}T$, and stage 2 (Figure 2b) during $NT + dT + d_{22}T < t \le NT + T$.

3. Modeling and Theoretical Analysis

Based on the averaging method in [19], the averaged model for the proposed step-up converter under the three cases are established and analyzed. Firstly, some symbols are defined. x is defined as the variables of the proposed step-up converter, such as i_{L1}, i_{L2}, i_{L3}, v_{C1}, v_0, d, and v_{in}. $\langle x \rangle$, X and $\hat{x}$ are denoted by their averaged, DC and small AC values, respectively. Also, the following items are assumed:

$$
\langle x \rangle = X + \hat{x} \ with \ \hat{x} << X
\tag{5}
$$

3.1. Averaged Model

3.1.1. Case 1: $L_1 = L_2$

For this case, $L_1 = L_2$ so that $i_{L1} = i_{L2}$. From (1) and (2), and using the averaging method in [19], the averaged model of the proposed step-up converter in case 1 can be directly derived as follows:

$$
\begin{cases}
\frac{d\langle i_{L1} \rangle}{dt} = \frac{\langle v_{in} \rangle + \langle v_{C1} \rangle}{L_1} d + \frac{\langle v_{in} \rangle - \langle v_0 \rangle}{2L_1}(1 - d) \\
\frac{d\langle i_{L3} \rangle}{dt} = -\frac{\langle v_{C1} \rangle}{L_3} + \frac{\langle v_0 \rangle (1 - d)}{L_3} \\
\frac{d\langle v_{C1} \rangle}{dt} = -\frac{2\langle i_{L1} \rangle}{C_1} d + \frac{\langle i_{L3} \rangle}{C_1} \\
\frac{d\langle v_0 \rangle}{dt} = \frac{\langle i_{L1} \rangle}{C_2}(1 - d) - \frac{\langle i_{L3} \rangle}{C_2}(1 - d) - \frac{\langle v_0 \rangle}{RC_2}
\end{cases}
\tag{6}
$$

3.1.2. Case 2: $L_1 < L_2$

As described in Section 2, there are three stages of the proposed step-up converter in case 2. The typical time-domain waveforms for the inductor currents i_{L1} and i_{L2} and the PWM signal v_d are plotted in Figure 3, where I_{LN}, I_{LM}, and I_{LN1} are the values of i_{L1} and i_{L2} at $t = NT$, $t = (N + d + d_{11})T$, and $t = (N + 1)T$, respectively, and I_{L1P} is the value of i_{L1} at $t = (N + d + d_{11})T$.

Based on (1), (2), (3), and Figure 3 and using the geometrical technique, the following equations can be derived:

$$
\frac{\langle v_{in} \rangle + \langle v_{C1} \rangle}{L_1} dT + \frac{\langle v_{in} \rangle - \langle v_0 \rangle}{L_1} d_{11}T = \frac{\langle v_{in} \rangle + \langle v_{C1} \rangle}{L_2} dT
\tag{7}
$$

$$
\langle i_{L1} \rangle = \frac{I_{LN} + I_{L1P}}{2} d + \frac{I_{L1P} + I_{LM}}{2} d_{11} + \frac{I_{LM} + I_{LN1}}{2}(1 - d - d_{11})
\tag{8}
$$

$$
\langle i_{L2} \rangle = \frac{I_{LN} + I_{LM}}{2} d + I_{LM} d_{11} + \frac{I_{LM} + I_{LN1}}{2}(1 - d - d_{11})
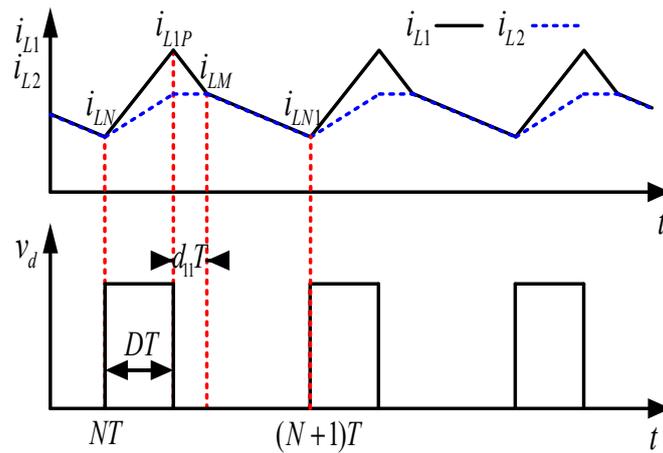\tag{9}
$$

Figure 3. Typical time-domain waveforms about i_{L1}, i_{L2} and v_d for the proposed step-up converter under $L_1 < L_2$.

Hence, the expressions for d_{11} and $\langle i_{L2} \rangle$ can be derived as follows:

$$d_{11} = \frac{(\langle v_{in} \rangle + \langle v_{C1} \rangle)L_1 Kd}{\langle v_0 \rangle - \langle v_{in} \rangle} \tag{10}$$

$$\langle i_{L2} \rangle = \langle i_{L1} \rangle - (\langle v_{in} \rangle + \langle v_{C1} \rangle + \frac{(\langle v_{in} \rangle + \langle v_{C1} \rangle)^2 L_1 K}{\langle v_0 \rangle - \langle v_{in} \rangle}) \frac{Kd^2}{2f} \tag{11}$$

where $K = 1/L_1 - 1/L_2$. Thereby, the completed averaged model of the proposed step-up converter in case 2 can be obtained by using the averaging method in (1)–(3), and then combining (10) and (11). The result is:

$$\begin{cases} \frac{d\langle i_{L1} \rangle}{dt} = \frac{\langle v_{in} \rangle + \langle v_{C1} \rangle}{L_1 + L_2} 2d + \frac{\langle v_{in} \rangle - \langle v_0 \rangle}{L_1 + L_2}(1 - d) \\ \frac{d\langle i_{L3} \rangle}{dt} = -\frac{\langle v_{C1} \rangle}{L_3}d + \frac{\langle v_0 \rangle - \langle v_{C1} \rangle}{L_3}(1 - d) \\ \frac{d\langle v_{C1} \rangle}{dt} = \frac{\langle i_{L3} \rangle}{C_1} - 2\frac{\langle i_{L1} \rangle}{C_1}d + \frac{Kd^3}{2fC_1}(\langle v_{in} \rangle + \langle v_{C1} \rangle - \frac{(\langle v_{in} \rangle + \langle v_{C1} \rangle)^2 L_1 K}{\langle v_{in} \rangle - \langle v_0 \rangle}) \\ \frac{d\langle v_0 \rangle}{dt} = -\frac{\langle v_0 \rangle}{RC_2} + (\frac{\langle i_{L1} \rangle}{C_2} - \frac{\langle i_{L3} \rangle}{C_2})(1 - d) \end{cases} \tag{12}$$

3.1.3. Case 3: $L_1 > L_2$

As indicated in Section 2, for case 3, the proposed step-up converter also has three stages, and its typical domain waveforms are shown in Figure 4, where I_{LN}, I_{LM}, and I_{LN1} are the values of i_{L1} and i_{L2} at $t = NT$, $t = (N + d + d_{22})T$ and $t = (N + 1)T$, respectively, and I_{L2P} is the value of i_{L2} at $t = (N + d + d_{22})T$. Because case 3 is similar to case 2, the completed averaged model of the proposed step-up converter for case 3 is directly derived as follows:

$$\begin{cases} \frac{d\langle i_{L2} \rangle}{dt} = \frac{\langle v_{in} \rangle + \langle v_{C1} \rangle}{L_2 + L_1} 2d + \frac{\langle v_{in} \rangle - \langle v_0 \rangle}{L_2 + L_1}(1 - d) \\ \frac{d\langle i_{L3} \rangle}{dt} = -\frac{\langle v_{C1} \rangle}{L_3}d + \frac{\langle v_0 \rangle - \langle v_{C1} \rangle}{L_3}(1 - d) \\ \frac{d\langle v_{C1} \rangle}{dt} = \frac{\langle i_{L3} \rangle}{C_1} - 2\frac{\langle i_{L2} \rangle}{C_1}d - \frac{Kd^3}{2fC_1}(\langle v_{in} \rangle + \langle v_{C1} \rangle + \frac{(\langle v_{in} \rangle + \langle v_{C1} \rangle)^2 L_2 K}{\langle v_{in} \rangle - \langle v_0 \rangle}) \\ \frac{d\langle v_0 \rangle}{dt} = -\frac{\langle v_0 \rangle}{RC_2} + (\frac{\langle i_{L2} \rangle}{C_2} - \frac{\langle i_{L3} \rangle}{C_2})(1 - d) \end{cases} \tag{13}$$
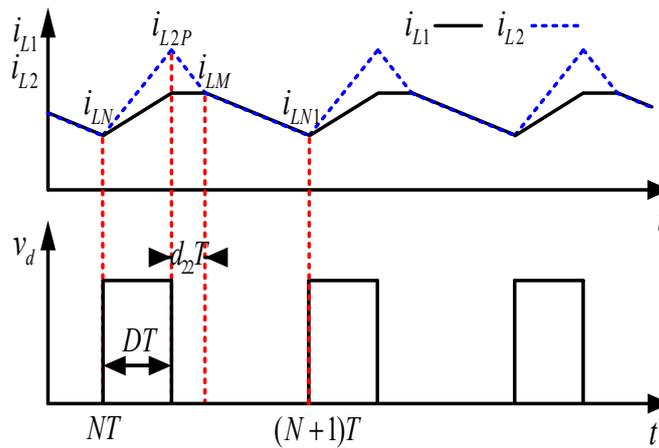
Figure 4. Typical time-domain waveforms about i_{L1}, i_{L2} and v_d for the proposed step-up converter under $L_1 > L_2$.

3.2. DC Equilibrium Point

By substituting (5) into (6), (12), and (13), and then separating DC items, the DC equilibrium points of the proposed step-up converter under three cases can be derived; they are shown in Table 1.

Table 1. DC equilibrium points of proposed step-up converter.

Items	Case 1: $L_1 = L_2$	Case 2: $L_1 < L_2$	Case 3: $L_1 > L_2$
I_{L1}	$\frac{M^2 V_{in}}{R(1+D)}$	$\frac{M^2 V_{in}}{R(1+D)} + K_1 I_{L0}$	$\frac{M^2 V_{in}}{R(1+D)} - K_4 I_{L0}$
I_{L2}	$\frac{M^2 V_{in}}{R(1+D)}$	$\frac{M^2 V_{in}}{R(1+D)} + K_2 I_{L0}$	$\frac{M^2 V_{in}}{R(1+D)} - K_3 I_{L0}$
I_{L3}	$\frac{2M^2 D V_{in}}{R(1+D)}$	$\frac{2M^2 D V_{in}}{R(1+D)} + K_1 I_{L0}$	$\frac{2M^2 D V_{in}}{R(1+D)} - K_3 I_{L0}$
V_{C1}	$\frac{1+D}{1-2D} V_{in}$	$\frac{1+D}{1-2D} V_{in}$	$\frac{1+D}{1-2D} V_{in}$
V_0	$M V_{in}$	$M V_{in}$	$M V_{in}$

where $I_{L0} = K D^2 V_{in}/(4f(1 - 2D)^2)$, $K_1 = (D - 2)((D - 1)L_1/L_2 + 1 + D)$, $K_2 = K_1 - (2D + L_1 K(1 - D))(2 - D)$ $(1 - 2D)/D$, $K_3 = (D - 2)((D - 1)L_2/L_1 + 1 + D)$, $K_4 = K_3 - (2D - L_2 K(1 - D))(2 - D)(1 - 2D)/D$.

From Table 1, it can be seen that the expressions for the DC voltage V_0 under the three cases are equal. In other words, no matter what the relation between L_1 and L_2 is, the voltage conversion ratio M of the proposed step-up converter can be described as follows:

$$M = \frac{1 + D}{(1 - D)(1 - 2D)} \tag{14}$$

Also, the expressions for the DC voltage V_{C1} under three cases are also equal. In conclusion, the relation between L_1 and L_2 does not influence V_0 and V_{C1}.

3.3. Voltage Stress of Power Switches and Diodes under Three Cases

Based on the definition of the voltage stress on the power switch and diode, the corresponding results for the proposed step-up converter under the three cases can be derived; they are shown in Table 2. One can see that the voltage stresses on the power switches (Q_1 and Q_2) and diodes (D_2, D_4 and D_5) under the three cases are equal except for the diodes D_1 and D_3.

Table 2. Voltage stress on power switches and diodes.

Items	Case 1: $L_1 = L_2$	Case 2: $L_1 < L_2$	Case 3: $L_1 > L_2$
Q_1	MV_{in}	MV_{in}	MV_{in}
Q_2	$\frac{1+D}{1-2D}V_{in}$	$\frac{1+D}{1-2D}V_{in}$	$\frac{1+D}{1-2D}V_{in}$
D_1	$\frac{M-1}{2}V_{in}$	$(M-1)V_{in}$	$\frac{(M-1)L_1V_{in}}{L_1+L_2}$
D_2	$\frac{2-D}{1-2D}V_{in}$	$\frac{2-D}{1-2D}V_{in}$	$\frac{2-D}{1-2D}V_{in}$
D_3	$\frac{M-1}{2}V_{in}$	$\frac{(M-1)L_2V_{in}}{L_1+L_2}$	$(M-1)V_{in}$
D_4	$\frac{1+D}{1-2D}V_{in}$	$\frac{1+D}{1-2D}V_{in}$	$\frac{1+D}{1-2D}V_{in}$
D_5	$(2-D)MV_{in}$	$(2-D)MV_{in}$	$(2-D)MV_{in}$

3.4. Ripples for Inductor Currents and Capacitor Voltages

The ripples for the inductor currents and the capacitor voltages can be obtained by using (1) and Table 1. The results are shown in Table 3.

Table 3. Ripples for inductor currents and capacitor voltages.

Items	Case 1: $L_1 = L_2$	Case 2: $L_1 < L_2$	Case 3: $L_1 > L_2$
Δi_{L1}	$\frac{D(2-D)TV_{in}}{(1-2D)L_1}$	$\frac{D(2-D)TV_{in}}{(1-2D)L_1}$	$\frac{D(2-D)TV_{in}}{(1-2D)L_1}$
Δi_{L2}	$\frac{D(2-D)TV_{in}}{(1-2D)L_2}$	$\frac{D(2-D)TV_{in}}{(1-2D)L_2}$	$\frac{D(2-D)TV_{in}}{(1-2D)L_2}$
Δi_{L3}	$\frac{D(1+D)TV_{in}}{(1-2D)L_3}$	$\frac{D(1+D)TV_{in}}{(1-2D)L_3}$	$\frac{D(1+D)TV_{in}}{(1-2D)L_3}$
Δv_{C1}	$\frac{2(1-D)M^2V_{in}}{R(1+D)C_1}DT$	$\left(\frac{2(1-D)M^2V_{in}}{R(1+D)} + K_2I_{L0}\right)\frac{DT}{C_1}$	$\left(\frac{2(1-D)M^2V_{in}}{R(1+D)} - K_4I_{L0}\right)\frac{DT}{C_1}$
Δv_0	$\frac{MV_{in}DT}{RC_2}$	$\frac{MV_{in}DT}{RC_2}$	$\frac{MV_{in}DT}{RC_2}$

Hence, unlike the voltage ripple for capacitor C_1, the current ripples for inductors (L_1, L_2 and L_3) and the voltage ripples for capacitor C_2 under the three cases are equal. Generally, the ripple ratio, which is defined by the ripple over the corresponding DC value, can be used to select the values of the inductors and capacitors.

3.5. Transfer Functions

The transfer function is fundamental for the consequent controller design for DC-DC converters. By substituting (5) into (6), (12), and (13), and then separating AC items and ignoring the second- and higher-order AC terms because their values are very small, the corresponding transfer functions for the proposed step-up converter under the three cases can be derived by using their respective definitions.

The control-to-output voltage transfer function $G_{vd}(s)$, the input voltage-to-output voltage transfer function $G_{vv}(s)$, the control-to-inductor current i_{L1} transfer function $G_{i1d}(s)$, and the input voltage-to-inductor current i_{L1} transfer function $G_{i1v}(s)$ of the proposed step-up converter can be obtained as follows:

$$G_{vd}(s) = \left.\frac{\hat{v}_0(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0} = [0,\,0,\,0,\,1](s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_d \tag{15}$$

$$G_{vv}(s) = \left.\frac{\hat{v}_0(s)}{\hat{v}_{in}(s)}\right|_{\hat{d}(s)=0} = [0,\,0,\,0,\,1](s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_v \tag{16}$$

$$G_{i1d}(s) = \left.\frac{\hat{i}_{L1}(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0} = [1,\,0,\,0,\,0](s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_d \tag{17}$$

$$G_{i1v}(s) = \left.\frac{\hat{i}_{L1}(s)}{\hat{v}_{in}(s)}\right|_{\hat{d}(s)=0} = [1,\,0,\,0,\,0](s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}_v \tag{18}$$

where the expressions for $\mathbf{A}$, $\mathbf{B}_d$ and $\mathbf{B}_v$ under the three cases are presented in Table 4.

Table 4. Expressions for **A**, $\mathbf{B_d}$ and $\mathbf{B_v}$ for the proposed step-up converter.

Case	A	$\mathbf{B_d}$	$\mathbf{B_v}$
Case 1: $L_1 = L_2 = L$	$\begin{bmatrix} 0 & 0 & \frac{D}{L} & \frac{D-1}{2L} \\ 0 & 0 & -\frac{1}{L_3} & \frac{1-D}{L_3} \\ -\frac{2D}{C_1} & \frac{1}{C_1} & 0 & 0 \\ \frac{1-D}{C_2} & \frac{D-1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix}$	$\begin{bmatrix} \frac{1+3M-2MD}{2L}V_{in} \\ -\frac{M}{L_3}V_{in} \\ -\frac{2M^2V_{in}}{RC_1(1+D)} \\ -\frac{(1-2D)M^2V_{in}}{RC_2(1+D)} \end{bmatrix}$	$\begin{bmatrix} \frac{1+D}{2L} \\ 0 \\ 0 \\ 0 \end{bmatrix}$
Case 2: $L_1 < L_2$	$\begin{bmatrix} 0 & 0 & \frac{2D}{L_1+L_2} & \frac{D-1}{L_1+L_2} \\ 0 & 0 & -\frac{1}{L_3} & \frac{1-D}{L_3} \\ -\frac{2D}{C_1} & \frac{1}{C_1} & \frac{\alpha_2}{C_1} & \frac{\alpha_2}{C_1} \\ \frac{1-D}{C_2} & \frac{D-1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix}$	$\begin{bmatrix} \frac{1+3M-2MD}{L_1+L_2}V_{in} \\ -\frac{M}{L_3}V_{in} \\ \frac{\beta_2}{C_1} \\ -\frac{(1-2D)M^2V_{in}}{RC_2(1+D)} \end{bmatrix}$	$\begin{bmatrix} \frac{1+D}{L_1+L_2} \\ 0 \\ \frac{KD^3(L_1K\beta_4-1)}{2fC_1} \\ 0 \end{bmatrix}$
Case 3: $L_1 > L_2$	$\begin{bmatrix} 0 & 0 & \frac{2D}{L_1+L_2} & \frac{D-1}{L_1+L_2} \\ 0 & 0 & -\frac{1}{L_3} & \frac{1-D}{L_3} \\ -\frac{2D}{C_1} & \frac{1}{C_1} & \frac{\alpha_3}{C_1} & \frac{\alpha_3}{C_1} \\ \frac{1-D}{C_2} & \frac{D-1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix}$	$\begin{bmatrix} \frac{1+3M-2MD}{L_1+L_2}V_{in} \\ -\frac{M}{L_3}V_{in} \\ \frac{\beta_3}{C_1} \\ -\frac{(1-2D)M^2V_{in}}{RC_2(1+D)} \end{bmatrix}$	$\begin{bmatrix} \frac{1+D}{L_1+L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix}$

where $\alpha_2 = KD^3(1 - M - 2L_1K(1 + M - MD))/(2f(1 - M))$, $\alpha_3 = -KD^3(1 - M + 2L_2K(1 + M - MD))/(2f(1 - M))$,
$\beta_2 = -2M^2V_{in}/(R(1 + D)) - 2K_1I_{L0} + 3D^2KV_{in}(1 + M(1 - D))(1 - L_1K(1 + M(1 - D))/(1 - M))/(2f)$,
$\beta_3 = -2M^2V_{in}/(R(1 + D)) + 2K_3I_{L0} - 3D^2KV_{in}(1 + M(1 - D))(1 + L_2K(1 + M(1 - D))/(1 - M))/(2f)$,
$\beta_4 = (2(1 + M(1 - D))(1 - M) - (1 + M)^2)/(1 - M)^2$.

4. Comparisons among Different Topologies

Table 5 shows the comparisons among the modified Sheppard-Taylor converter (MSTC) in [14], the PWM Z-source DC-DC converter (ZSC) in [18], the simple modified Sheppard-Taylor converter (SMSTC) in [15], and the proposed step-up converter (PSUC).

Table 5. Comparisons among the converters.

Topology	MSTC in [14]	ZSC in [18]	SMSTC in [15]	PSUC
M	$\frac{D}{(1-D)(1-2D)}$	$\frac{1-D}{1-2D}$	$\frac{1}{1-2D}$	$\frac{1+D}{(1-D)(1-2D)}$
Switches	2	1	2	2
Diodes	4	1	3	5
Inductors	2	3	1	3
Capacitors	2	3	2	2
Output floating	No	Yes	No	No

Although the proposed step-up converter has five diodes, while others have less, from Figure 5, which shows the comparisons of the voltage conversion ratio M among these converters under different duty cycle D, it can be seen that the proposed step-up converter possesses the highest voltage conversion ratio. For example, the voltage conversion ratio M of the proposed step-up converter is up to 46.224 at $D = 0.47$. Additionally, the ZSC's output voltage is floating, whereas those of the others are not.
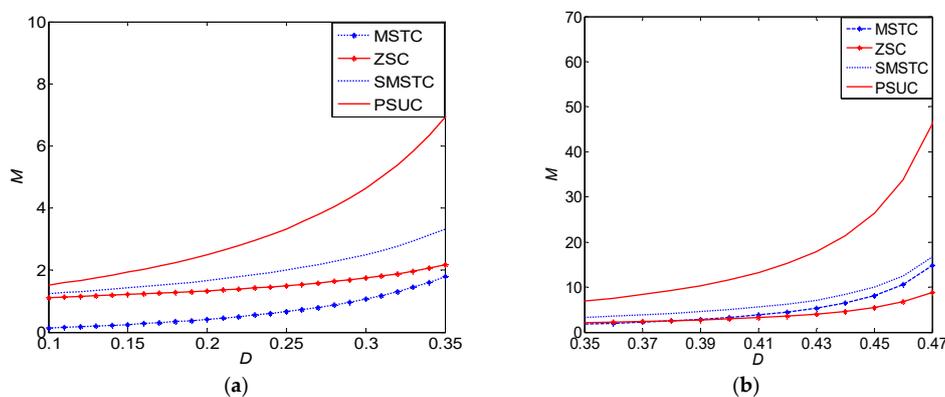

Figure 5. Comparisons about the voltage conversion ratio M among MSTC, ZSC, SMSTC and PSUC. (**a**) D is within 0.1–0.35; (**b**) D is within 0.35–0.47.

5. Saber Simulations and Circuit Experiments

For validation purposes, the circuit for the proposed step-up converter is designed. The given specifications are described as V_{in} = 12 V, V_0 = 90 V, f = 32 kHz, R = 300 Ω. Thus, from (14), the duty cycle D should be equal to 0.358742. Based on the voltage stresses of the power switches and diodes in Table 2, the HEXFET Power MOSFET IRFP4668 whose V_{DSS} = 200 V was selected for power switches Q_1 and Q_2, and the Switchmode Schotty Power Rectifier MBR40250 rated for 250 V was selected for diodes D_1, D_2, D_3, D_4, and D_5. Inductors (L_1, L_2 and L_3) can be designed by using their current ripple ratios $\varepsilon_L = \Delta i_L / I_L$ whose values should generally be less than 45%. Capacitors C_1 and C_2 can be designed by using their voltage ripple ratios $\varepsilon_C = \Delta v_C / V_C$ whose values should be less than 20% and 0.5%, respectively. Thereby, from Tables 1 and 3, the current ripple ratio for each inductor and the voltage ripple ratio for each capacitor under each case can be calculated, and accordingly the selected inductors and capacitors in each case should satisfy conditions: L_1 > 1048 μH, L_2 > 1048 μH, L_3 > 1210 μH, C_1 > 2.06 μF and C_2 > 7.47 μF. Here, C_1 = 4.7 μF with r_{C1} = 10 mΩ, C_2 = 40 μF with r_{C2} = 6 mΩ, and L_3 = 2.76 mH with r_{L3} = 164 mΩ were selected for the proposed step-up converter. Additionally, L_1 = L_2 = 1.2 mH with r_{L1} = r_{L2} = 70 mΩ were selected for case 1, L_1 = 1.2 mH with r_{L1} = 70 mΩ and L_2 = 2.27 mH with r_{L2} = 156 mΩ were selected for case 2, and L_1 = 2.27 mH with r_{L1} = 156 mΩ and L_2 = 1.2 mH with r_{L2} = 70 mΩ were selected for case 3.

From the above-designed circuit parameters, the simulated model in Saber software, which is widely used in the field of power electronics [20], for the proposed step-up converter is constructed, and some measured results on the output voltage V_0 from the saber simulations were presented in Table 6. One can see that the output voltages V_0 for the proposed step-up converter in the three cases were close, and their values were smaller than the required 90 V because the parasitic parameters were considered in the Saber simulations.

Table 6. Comparisons of the output voltage V_0 between the calculations and the saber simulations.

Cases	$L_1 = L_2$	$L_1 < L_2$	$L_1 > L_2$
Calculations for V_0	90.000 V	90.000 V	90.000 V
Simulations for V_0	84.217 V	83.362 V	83.363 V

Moreover, a hardware circuit for the proposed step-up converter with the same circuit parameters and selected power switches and diodes was also constructed. Notably, in the experiments, the photocoupler TLP250H was applied to drive the power switches. The averaged values of the input voltage V_{in}, the input current I_{in} and the output voltage V_0 with different duty cycle D for the proposed step-up converter under case 1 were measured. In addition, then, the voltage conversion ratio $M = V_0/V_{in}$ and the efficiency $\eta = V_0^2/(RV_{in}I_{in})$ with different duty cycle D for the proposed step-up converter in case 1 were calculated and plotted in Figure 6a,b, respectively. Simultaneously, the corresponding Saber simulations were also detected, calculated, and plotted in Figure 6a,b. It can be seen that the experimental results were in basic agreement with the Saber simulations.

As shown in Table 6, it is necessary to design an appropriate controller for this proposed step-up converter. Based on the circuit parameters, the zeros of $G_{vd}(s)$ (shown in (15)) can be calculated. The results showed that $G_{vd}(s)$ was a fourth-order and non-minimum phase since it had right-half side zeros, so that it was difficult to select only the single voltage loop to obtain good performance [21]. Alternatively, an average current mode controller shown in Figure 7 was selected and designed for the proposed step-up converter. This controller had an outer voltage loop and an inner current loop. For the outer voltage loop, it was necessary to detect the output voltage v_0 and design a voltage compensator. For the inner current loop, it was necessary to select one of the inductor currents in the proposed step-up converter and design a current compensator. Due to all the $G_{i1d}(s)$'s poles and zeros being in the left-half side of the s-plane, that is, $G_{i1d}(s)$ is stable and minimum phase, the inductor current i_{L1} was selected and measured for the average current mode controller. Notably, the inductor current i_{L1} here was transformed into a voltage with the same value through the current

transducer LA55-A. The current compensator's output voltage is denoted by v_{vi}. AM1 and AM2 were realized by the operational amplifiers LF356 and COM was realized by the voltage comparator LM311. The corresponding parameters were: R_{vi} = 1000 kΩ, R_{vd} =20 kΩ, R_{vf} = 200 kΩ, C_{vf} = 10 nF, R_i = 20 kΩ, R_p = 180 kΩ, C_p = 10 nF, C_i = 100 pF, V_{ref} = 1.76 V. The PWM signal v_d was generated by comparing the voltage v_{vi} with the ramp signal V_{ramp}, whose expression was given as follows:

$$V_{ramp} = V_L + (V_U - V_L)\left(\frac{t}{T}\bmod 1\right) \tag{19}$$

where V_L = 0 V, V_U = 10 V and $T = 1/f$.
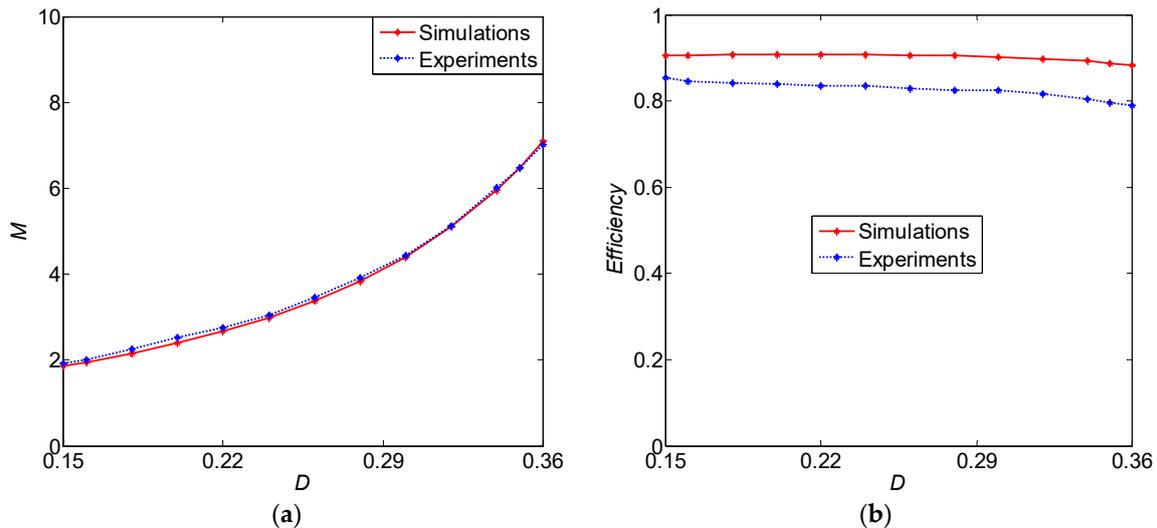
Figure 6. The Saber simulations and the experiments about the voltage conversion ratio *M* and the efficiency for the proposed step-up converter under case 1. (**a**) The voltage conversion ratio *M*; (**b**) The efficiency.
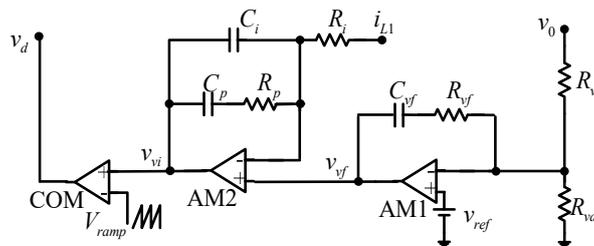
Figure 7. Circuit schematic for the average current mode controller.

The experimental results for the output voltage v_0, the inductor currents i_{L1} and i_{L2}, and the PWM signal v_d for the average-current mode controlled proposed step-up converter under the three cases are presented in Figure 8a–c, respectively. One can see that the output voltages v_0 for the systems under the three cases are really the same, despite different relations between the inductors L_1 and L_2. Moreover, the response of the output voltage v_0, the inductor current i_{L1}, and the PWM signal v_d for the average-current mode controlled proposed step-up converter with the step changing of the load *R* being 300 Ω–600 Ω–300 Ω is shown in Figure 9. One can see that the closed-loop controlled proposed step-up converter had good performance.
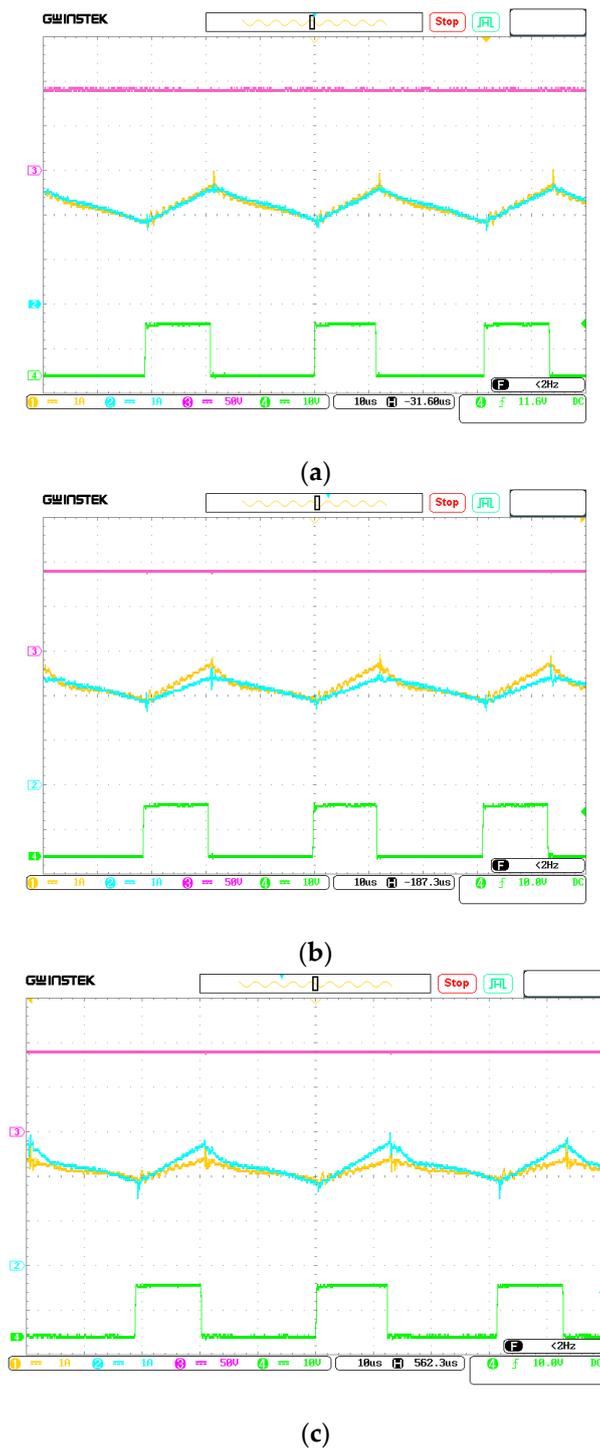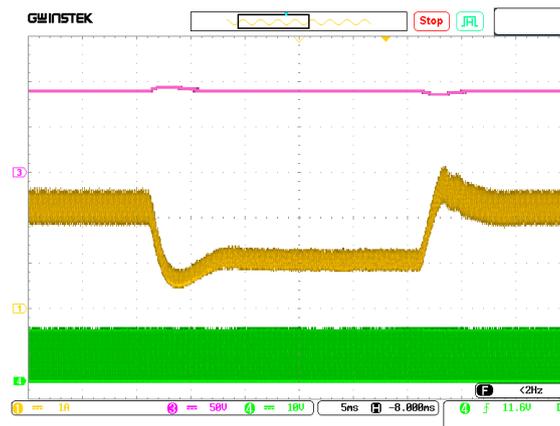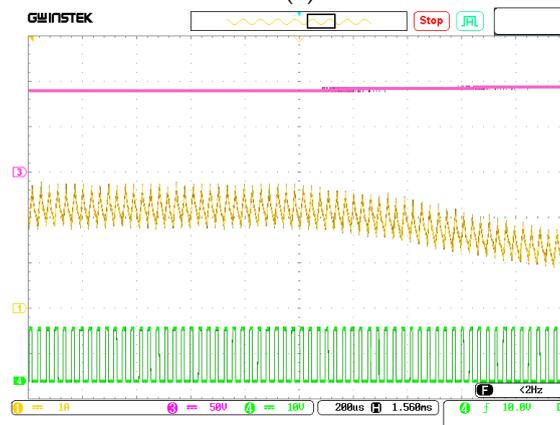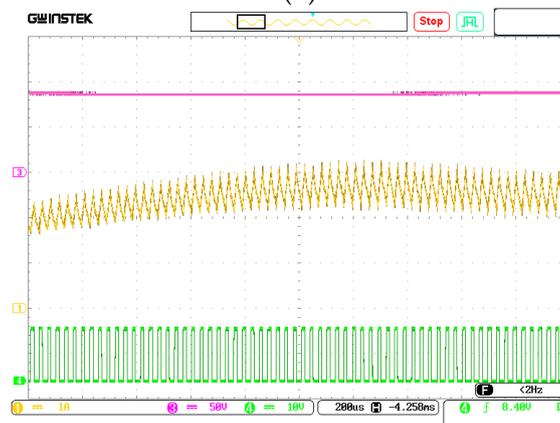
(**a**)

(**b**)

(**c**)

Figure 8. Experimental results for v_0 (Top: 50 V/div, Pink), i_{L1} (Middle: 1 A/div, Yellow), i_{L2} (Middle: 1 A/div, Blue) and v_d (Bottom: 10 V/div, Green) for the average current mode controlled proposed step-up converter under three cases. (**a**) Case 1: L_1 = 1.2 mH and L_2 = 1.2 mH; (**b**) Case 2: L_1 = 1.2 mH and L_2 = 2.27 mH; (**c**) Case 3: L_1 = 2.27 mH and L_2 = 1.2 mH.

(**a**)

(**b**)

(**c**)

Figure 9. Response of v_0 (Top: 50 V/div, Pink), i_{L1} (Middle: 1 A/div, Yellow) and v_d (Bottom: 10 V/div, Green) with the step change of the resistive load R being 300 Ω–600 Ω–300 Ω. (**a**) Time: 5 ms/div; (**b**) Close-up view of response for the step changing of the resistive load R being 300 Ω–600 Ω, Time: 200 μs/div; (**c**) Close-up view of response for the step changing of the load R being 600 Ω–300 Ω, Time: 200 μs/div.

6. Conclusions

This paper introduces a new step-up converter. The results from theoretical analysis, the Saber simulations, and the circuit experiments show that, even if it has five diodes and five storage elements, it still has the following five good features:

(1) Although this new step-up converter has five storage elements, that is, three inductors and two capacitors, its averaged model is still fourth-order, because one of the input inductor currents can be expressed by another input inductor current.

(2) The relation between the inductor L_1 and L_2 has three cases: $L_1 = L_2$, $L_1 < L_2$, and $L_1 > L_2$. However, these relations do not influence its output voltage V_0, i.e., the output voltage V_0 are the same in the three cases.

(3) Compared to MSTC, ZSC, and SMSTC, the proposed step-up converter has ultrahigh voltage conversion ratio.

(4) The output voltage of the proposed step-up converter is common-ground and common-polarity with its input voltage, so its value is easy to detect.

(5) The proposed step-up converter has no abrupt changes in capacitor voltage and inductor current, so it does not suffer from infinite capacitor current and inductor voltage.

Thus, the proposed step-up converter with ultrahigh voltage conversion ratio is a good candidate topology for applications of photovoltaic systems and fuel cell systems, and these applications will be investigated in future work.

Nomenclature of Main Symbols and Variables

Q_1, Q_2	Power mosfets
D_1, D_2, D_3, D_4, D_5	Power Diodes
L_1, L_2, L_3 (mH)	Inductors of power stage
C_1, C_2 (μF)	Capacitors of power stage
R (Ω)	Resistive load
V_{ramp}	Ramp signal
v_d (V)	PWM signal
f (kHz)	Switching frequency
$d, D, \hat{d}$	Instantaneous, DC and small signal of duty cycle
$v_{in}, V_{in}, \hat{v}_{in}$ (V)	Instantaneous, DC and small signal of input voltage
T (μs)	Switching period
i_{L1}, i_{L2}, i_{L3} (A)	Instantaneous values of inductor currents
I_{L1}, I_{L2}, I_{L3} (A)	DC values of inductor currents
$\langle i_{L1} \rangle, \langle i_{L2} \rangle, \langle i_{L3} \rangle$ (A)	Averaged values of inductor currents
$\hat{i}_{L1}, \hat{i}_{L2}, \hat{i}_{L3}$ (A)	Small signal of inductor currents
$\Delta i_{L1}, \Delta i_{L2}, \Delta i_{L3}$ (A)	Ripples of inductor currents
v_{C1}, v_0 (V)	Instantaneous values of capacitor voltage of C_1, C_2
$\langle v_{C1} \rangle, \langle v_0 \rangle$ (V)	Averaged values of capacitor voltage of C_1, C_2
V_{C1}, V_0 (V)	DC values of capacitor voltage of C_1, C_2
$\hat{v}_{C1}, \hat{v}_0$ (V)	Small signal of capacitor voltage of C_1, C_2
$\Delta v_{C1}, \Delta v_0$ (V)	Ripples of capacitor voltage of C_1, C_2

$G_{vd}(s)$	Control-to-output voltage transfer function
$G_{vv}(s)$	Input voltage-to-output voltage transfer function
$G_{i1d}(s)$	Control-to-inductor current i_{L1} transfer function
$G_{i1v}(s)$	Input voltage-to-inductor current i_{L1} transfer function
$R_{vi}, R_{vd}, R_{vf}, R_i, R_p$ (kΩ)	Resistors of average current mode controller
C_{vf}, C_p, C_i (μF)	Capacitors of average current mode controller
V_{ref} (V)	Reference voltage
V_L, V_U (V)	Lower and upper threshold of ramp signal

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