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Performance Improvement for Reduction of Resonance in a Grid-Connected Inverter System Using an Improved DPWM Method

Jin-Hyuk Park and Kyo-Beum Lee *

Department of Electrical and Computer Engineering, Ajou University, 206, World cup-ro, Yeongtong-gu, Suwon 16499, Korea; powerword87@gmail.com

* Correspondence: kyl@ajou.ac.kr; Tel.: +82-31-219-2487

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Abstract: This paper proposes discontinuous pulse width modulation (DPWM) for a grid-connected inverter system using an LCL-filter which consists of two inductors and a capacitor that is connected in parallel per phase. The modulation signal is discontinuously changed, and the harmonic voltages are generated in the wide frequency range at the output terminal of the inverter when the conventional DPWM is used. If these harmonic voltages are present in the resonance frequency band by an LCL-filter, then the resonance problem of the grid current occurs. To suppress the resonance problem, the proposed DPWM injects the sixth harmonic to the modulation signal. Therefore, in the improved DPWM, harmonic voltages at the output terminal of the inverter are sufficiently reduced because the discontinuous change of the modulation signal disappears. The proposed DPWM method is verified by a Powersim (PSIM) simulation (Powersim Inc., Rockville, MD, USA) and experiments with a 3-kW neutral-point clamped (NPC)-type grid-connected inverter system.

Keywords: discontinuous PWM; NPC-type grid connected inverter; resonance current; LCL-filter

1. Introduction

Recently, there has been growing interest in renewable energy because of the depletion of natural resources and increasing environmental pollution from the use of fossil fuels and nuclear energy [1–3]. For these reasons, the use of grid-connected inverter systems for renewable energy sources has become an important topic [4,5]. High efficiency is required for the effective use of power conditioning systems (PCSs).

Many studies have been conducted to achieve high inverter efficiency. To obtain high efficiency, there are several methods, such as the use of topologies with higher efficiency, highly efficient devices, and modified pulse width modulation (PWM) techniques.

To increase the efficiency of the PCS, highly efficient topologies utilizing the zero-voltage switching (ZVS) techniques have been studied [6,7]. These topologies have advantages regarding the efficiency. However, to achieve the ZVS, the required auxiliary circuit and control method are complicated.

Research has been conducted to compare the performance of the Si-IGBT and SiC-MOSFET power devices [8,9]. Recently, the SiC-MOSFET has been used widely in inverter systems to achieve higher efficiency, because these high-efficient devices have the advantage of high-speed switching and low switching losses when compared with the Si-IGBT [10]. However, the efficiency increase by the device has limitation on the performance of the device. SiC-MOSFET is also more expensive than the Si-IGBT.

The modification of the PWM method is the easiest to increase efficiency. The continuous PWM (CPWM) and discontinuous PWM (DPWM) are widely used switching methods for the inverter control [5,11]. The Space Vector PWM (SVM) is a typical CPWM. The modulation signal of the SVM is continuously changed depending on the line frequency. On the other hand, the modulation signal of

the DPWM is discontinuously changed. The DPWM can be applied based on the sinusoidal PWM (SPWM). The modulation signal is generated by injecting the DPWM offset to the modulation signal of the SPWM. The switching loss of the devices is affected, depending on the switching method. The DPWM can reduce the switching loss because the switching device is not switched when the modulation signal is clamped to the DC-bus. Therefore, the DPWM can increase the efficiency of the inverter.

The Output voltage of the inverter has a lot of harmonics because of the discontinuous change, which depends on the switching states. To control the grid current sinusoidal waveform, the grid-connected filter is essentially required. The aim of this filter is to attenuate the harmonic components in the switching frequency band. Recently, in order to reduce the volume and the cost of the filter, an LC- or LCL-filter (one or two inductors and a capacitor that is connected in parallel per phase) is widely used instead of the L-filter. When using the LC- or the LCL-filter, the resonance frequency band is formed [12,13]. In the DPWM, many harmonic voltages are generated in the wide frequency range at the output terminal of the inverter. If these harmonic voltages are in the resonance frequency band, the grid current oscillates [14]. This problem adversely affects the quality of the current and increases the total harmonic distortion (THD).

The selective harmonic elimination PWM method has been conducted to reduce the harmonic voltage [15–17]. This method can minimize the switching loss, while reducing the desired harmonics. Once harmonics, which should be reduced, are determined, switching angles are also determined. In this case, unselected harmonics cannot be reduced. If harmonics in the resonance frequency band are selected, the oscillation problem of the grid current can be solved. However, the resonance frequency is affected by the grid impedance in grid-connected system [18]. Therefore, if the grid impedance is large, then the harmonics in the resonance frequency band cannot be reduced.

This paper proposes the improved DPWM method to solve the resonance problem. The proposed method injects the sixth harmonic to the modulation signal to reduce the harmonic voltages at the output terminal of the inverter. The attenuation of the harmonics in the resonance frequency band improves the quality of the output current. The proposed algorithm is verified by PSIM simulations and experiments using a 3-kW neutral-point clamped (NPC)-type grid-connected inverter system.

2. Description of Grid-Connected Inverter System

Figure 1 shows the construction of the grid-connected inverter system. This system is composed of an LCL-filter, NPC-type inverter, and DC-link. To transfer the power between the grid and the DC-link, the inverter controls the DC-link and the output current. To reduce the switching ripple of the current, the LCL-filter is used in this paper. The LCL-filter is typically used to reduce the size of the filter. The LCL-filter consists of two inductors and a capacitor that is connected in parallel per phase, as shown in Figure 1. In this case, the resonance frequency band is formed around the resonance frequency [16]. The resonance frequency is defined as

$$f_{resonance} = \frac{1}{2\pi}\sqrt{\left(L_i + L_g\right) / \left(L_i L_g C_f\right)} \tag{1}$$

where L_i is the inverter side inductor, L_g is the grid side inductor, and C_f is the filter capacitor.

The transfer function of the LCL-filter is represented as

$$G(s) = \frac{i(s)}{v(s)} = \frac{1}{L_i s}\frac{\left(s^2 + R_d C_f z_{LC}^2 s + z_{LC}^2\right)}{\left(s^2 + R_d C_f \omega_{res}^2 s + \omega_{res}^2\right)} \tag{2}$$

where ${z^2}_{LC} = 1/L_T C_f$, ${\omega^2}_{res} = L_T {z^2}_{LC}/L_i$, and $L_T = L_i + L_2$.

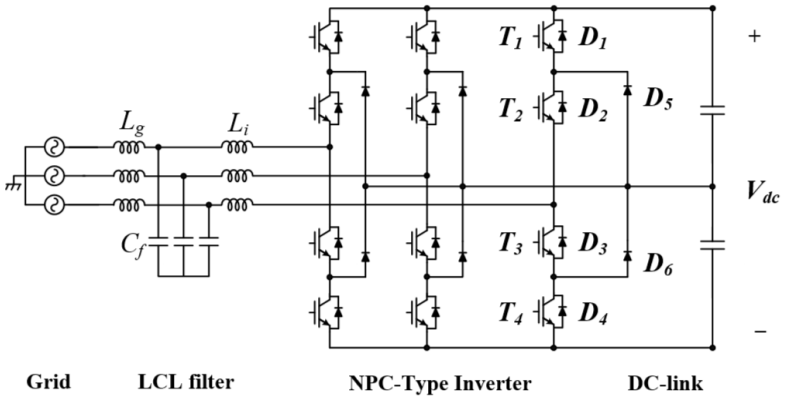


Figure 1. Circuit configuration of the grid-connected inverter system.

Figure 2 shows a Bode plot of the LCL-filter voltage and current. The LCL-filter parameters are the same as in the simulation condition. The magnitude of the LCL-filter gain is high at the resonance frequency.

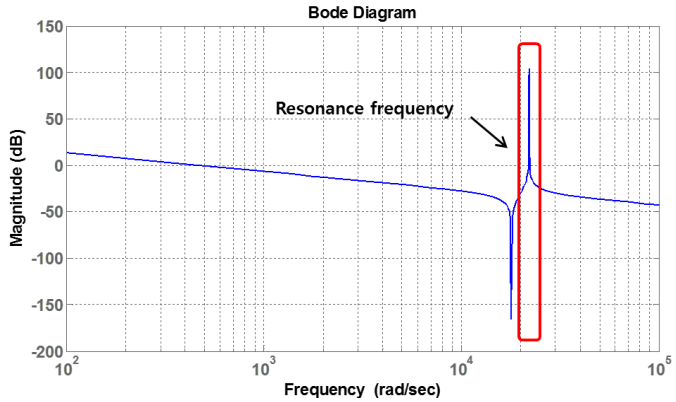


Figure 2. Bode plot of the LCL-filter as shown in Figure 1.

Figure 3 shows the control block of the grid-connected inverter. The dual loop control method is used to regulate the DC-link voltage in this paper. Outer loop is the DC-link controller and the inner loop is the current controller. The output of the outer loop is the reference of the active current for following the DC-link voltage reference. The inner loop can control the active and reactive components, respectively. The inverter that is used in this paper controls the power factor (PF) to 1. The inner loop is performed on the synchronous frame. The output of the inner loop is the dq-axis reference voltage (V^*_{dqe}). V^*_{dqe} changed to phase voltage reference (V^*_{abcs}) by inverse coordinate transformation. The phase angle used in inverse coordinate transformation is estimated by the phase locked loop (PLL). In grid-connected system, PLL follows the angle of the grid voltage. Therefore, V^*_{abcs} is synchronized with the grid voltage. 60° DPWM is implemented by the offset voltage with microprocessor. The offset voltage is calculated by maximum and minimum of V^*_{abcs}, as shown in Equation (4). The range where the maximum value among V^*_{abcs} is larger than the minimum value among V^*_{abcs} is 60°. In the opposite case, this range is 60°. Therefore, it is possible to implement 60° DPWM, according to the change of the offset voltage. The reference of the pole voltage is the sum of the reference of the phase voltage and the offset voltage. The PWM signal is generated by comparing the carrier signal and the pole voltage reference, which is the sum of the phase voltage reference and the offset voltage.

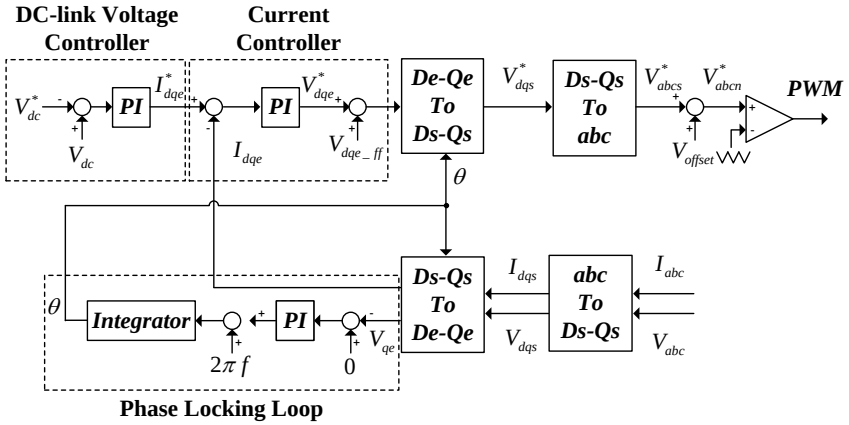


Figure 3. Control block diagram of the three-phase inverter with discontinuous PWM (DPWM).

3. Description of the Conventional 60° DPWM

In the DPWM, there are ranges where the switching devices maintain ON or OFF state. In these ranges, it is possible to reduce the switching loss of the switching devices because of the reduction of the switching amount. Therefore, the DPWM has the merit to increase the efficiency of the inverter by the reduction of the switching loss. In the grid-connected inverter systems, 60° DPWM are widely used among the several DPWM switching methods.

Figure 4 shows the reference and the offset voltage of the 60° DPWM. The pole voltage reference is used in the modulation signal and can be obtained by the sum of the phase voltage reference and the offset voltage. In this method, the switches of one-phase among three-phase maintain ON or OFF state every 60° range. The phase voltage references are used to determine the discontinuous range by comparing the amplitude of each phase voltage reference. These phase voltage reference (V^*_{as}, V^*_{bs}, $V^*_{cs} = V^*_{xs}$) are expressed as

$$\begin{aligned} V^*_{as} &= V_m \sin(\omega t) \\ V^*_{bs} &= V_m \sin(\omega t - 2\pi/3) \\ V^*_{cs} &= V_m \sin(\omega t + 2\pi/3) \end{aligned} \tag{3}$$

where V_m is the amplitude of the phase voltage reference and ω is the radian representation of 60 Hz fundamental frequency.

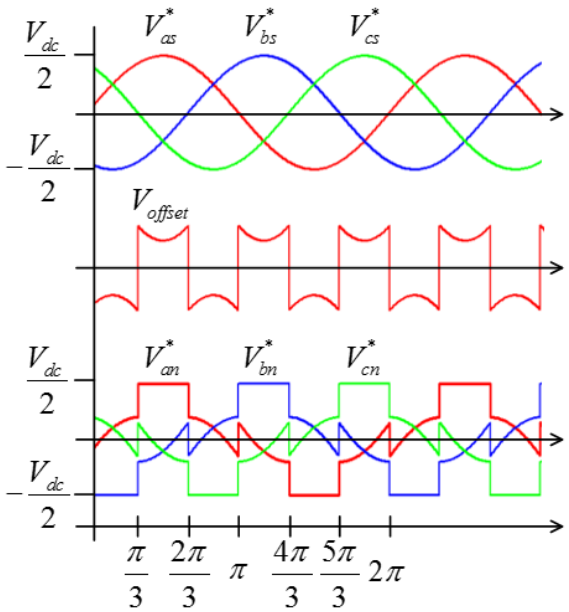


Figure 4. Voltage modulation signal of the 60° DPWM.

The offset voltage is obtained by the maximum and the minimum values of the V^*_{xs}. The offset voltage is expressed as

$$V_{offset} = \begin{cases} V_{dc}/2 - V_{\max} & |V_{\max}| \geq |V_{\min}| \\ -V_{dc}/2 - V_{\min} & |V_{\max}| \leq |V_{\min}| \end{cases} \quad (4)$$

where $V_{\max}$ is the maximum value and $V_{\min}$ is the minimum value among the V^*_{xs} and V_{dc} is the DC-link voltage.

The pole voltage reference can be obtained by the summation of V^*_{xs} and the V_{offset}. The references of the pole voltages (V^*_{an}, V^*_{bn}, $V^*_{cn} = V^*_{xn}$) are expressed as

$$V^*_{xn} = V^*_{xs} + V_{offset} \quad (5)$$

4. Analysis of the Resonance Problem with DPWM

In case of the DPWM switching method, V^*_{xn} are discontinuously changed because of the discontinuous variation of the offset voltage every 60° range. The output terminals of the inverter are clamped to the DC-bus, according to V^*_{xn}. Many harmonics at the output terminals are generated in the wide frequency range at the clamping moments of V^*_{xn}. If these harmonics are formed up to the resonance frequency band, harmonic voltages and resonance frequency band overlap. In this case, the grid currents oscillate at the clamping moment of V^*_{xn}.

In this paper, to analyze the output voltage harmonics, a numerical method is applied. When using this method, the harmonics can be approximated relatively easily. Figure 5 shows the V^*_{an}, carrier signal ($V_{carrier}$) and the switching function S_{SF}. The aim of applying the numerical method is to obtain the pattern of the S_{SF} to analyze the harmonic components of the inverter output voltage.

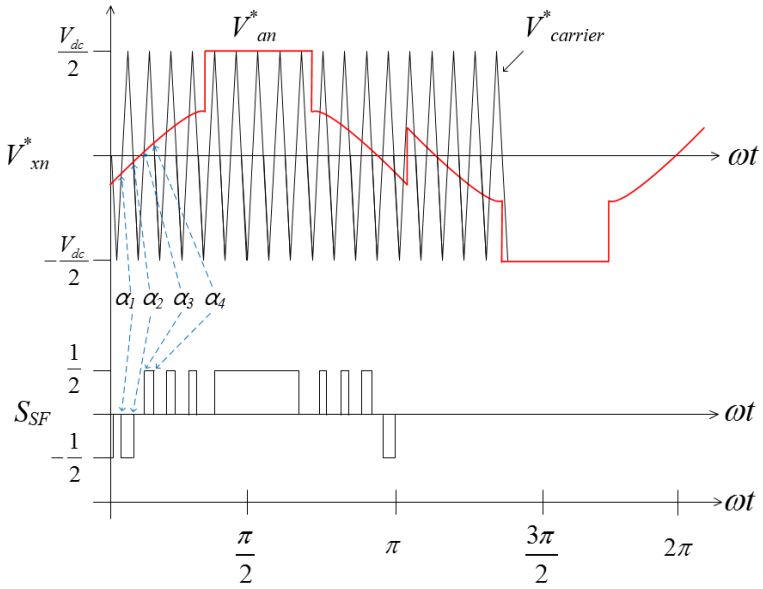


Figure 5. Switching angle and the switching function.

It is necessary to know the switching angle α_x to obtain the S_{SF} that has 0.5 or −0.5. α_x is determined by the intersection of V^*_{xn} and $V_{carrier}$. Therefore, α_x can be obtained from the equation representing the intersection of V^*_{xn} and $V_{carrier}$. For the convenience of analysis, this paper analyzes the harmonics in the following conditions.

(1) If m_f (switching frequency/line frequency) is odd, S_{SF} does not include even-order harmonics and has only odd-order harmonics.

(2) In this case, S_{SF} becomes the half-wave symmetrical and one cycle of the S_{SF} can be obtained by α_x between 0 and 90° (quarter cycle).

Figure 6 shows the method of determining the value of α_x. $V_{carrier}$ can be seen as the sum of the straight lines with the different slopes. Figure 6 represents the straight lines with different slopes, which are the solid line (L_{2i+1}) and dotted line (L_{2i}). All of the intersections of the solid lines and the dotted lines are $V_{dc}/2$ or $-V_{dc}/2$. Therefore, the distance between the straight lines having the same slope is expressed as

$$d = \frac{2\pi}{m_f} \tag{6}$$

From Equation (6), the slopes of the solid and the dotted lines are obtained as

$$S_L = \left\{ \begin{array}{cc} \frac{m_f}{\pi} V_{dc} & i = 1, 3, 5 \cdots 2n+1 \\ -\frac{m_f}{\pi} V_{dc} & i = 2, 4, 6 \cdots 2n \end{array} \right\} \tag{7}$$

From Equation (7), the equation of a line is determined to

$$L_i = (-1)^{i+1} \left[\frac{m_f}{\pi} V_{dc}(\omega t) - V_{dc} i \right] \tag{8}$$

Therefore, α_x can be obtained at the intersection of Equations (5) and (8). From Equations (5) and (8), when considering V^*_{an}, the equation for calculating α_x is follows as

$$V^*_{an} = (-1)^{i+1} \left[\frac{m_f}{\pi} V_{dc}(\omega t) - V_{dc} i \right] \tag{9}$$

The pattern of S_{SF} can be constructed through α_x obtained from Equation (9), as shown in Figure 5.

In this paper, to analyze the harmonic voltages at the output of the inverter, S_{SF} and the Fourier series are used. By considering the condition (1), the Fourier series can be expressed as

$$\begin{array}{c} a_0 = a_n = 0 \\ b_n = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} S_{SF} \sin(n\omega t) dt \end{array} \tag{10}$$

where n is only odd, and ω is the radian representation of 60 Hz; a_0, a_n, b_n are the Fourier series coefficients.

By substituting the pattern of S_{SF} into Equation (10), the magnitude of the harmonics is obtained as

$$b_n = \frac{2}{n\pi} \left[1 + 2 \sum_{j=1}^{k} (-1)^j \cos(n\alpha_j) \right] \tag{11}$$

where k is the number of the switching angle.

S_{SF} can be composed of the sum of all harmonics. Therefore, from Equation (11), S_{SF} is expressed as

$$S_{SF} = \sum_{n=1,3,5,\cdots}^{\infty} b_n \sin(n\omega t). \tag{12}$$

If considering the DC-bus voltage as S_{SF}, the output voltage of the inverter can be obtained. The variation of the output voltage is the half of the DC-bus voltage because the 3-level inverter is considered in this paper. Therefore, from Equation (12), the output voltage of the inverter is expressed as

$$V_o = S_{SF} V_{DC}/2 = \sum_{n=1,3,5,\cdots}^{\infty} (V_{DC}/2) b_n \sin(n\omega t) \tag{13}$$

From Equation (13), the harmonics magnitude of the output voltage is determined as

$$\hat{V}_n = \frac{V_{DC}}{n\pi}\left[1 + 2\sum_{j=1}^{k}(-1)^j \cos(n\alpha_j)\right]. \tag{14}$$

Equation (14) represents the harmonics magnitude of the *a*-phase output voltage. The harmonics magnitudes of the *b*-phase and the *c*-phase are the same as (14), but have a phase difference of 120°.

$$\begin{aligned} V_{o,a} &= \sum_{n=1,3,5,\cdots}^{\infty}(V_{DC}/2)b_n \sin(n\omega t) \\ V_{o,b} &= \sum_{n=1,3,5,\cdots}^{\infty}(V_{DC}/2)b_n \sin(n\omega t - 2\pi/3) \\ V_{o,c} &= \sum_{n=1,3,5,\cdots}^{\infty}(V_{DC}/2)b_n \sin(n\omega t + 2\pi/3) \end{aligned} \tag{15}$$

To investigate the cause of the resonance, the harmonic analysis of the phase voltage (V_{as}, V_{bs}, $V_{cs} = V_{xs}$) is required. V_{xs} is expressed as

$$\begin{aligned} V_{xs} &= V_{xn} + V_{sn} \\ V_{sn} &= (V_{o,a} + V_{o,b} + V_{o,c})/3 \end{aligned} \tag{16}$$

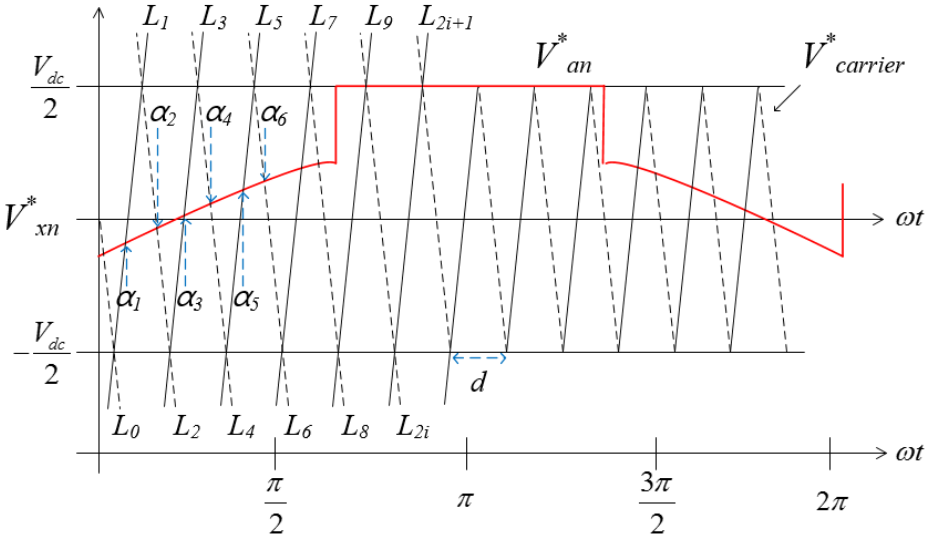


Figure 6. Determination of the switching angle.

Figure 7 shows the harmonics distribution of V_{xs} in simulation condition. To calculate the harmonic components of V_{xs}, Matlab simulation is used. From the above-mentioned conditions (1), the switching frequency is approximated to 7740 Hz for the convenience of the analysis, though the actual switching frequency applied in the experiment set is 7800 Hz. N = 1 and 129 harmonics are excluded in Figure 7 to see the distribution of the lower order harmonics in detail. The harmonics of the switching frequency band have the greatest magnitude. They are distributed in a wide band up to the lower order that is less than the half of the switching frequency. The harmonics in the resonance frequency band by LCL-filter can adversely affect the system because the gain is significant, as shown in Figure 2. When designing the LCL-filter, to ensure the stability of the system, the resonance frequency is placed in less than the half of the switching frequency to avoid the upper parts of the harmonic spectrum. However, when considering 60° DPWM switching method, the harmonics and the resonance frequency band are overlapped because the lower order harmonics exist in the resonance frequency band. It causes the resonance problem of the grid current. The low order harmonics below

the half of the switching frequency are generated at the moment when the modulation signal is clamped to the DC-bus. Consequently, the grid current oscillates every 60° in the conventional DPWM.

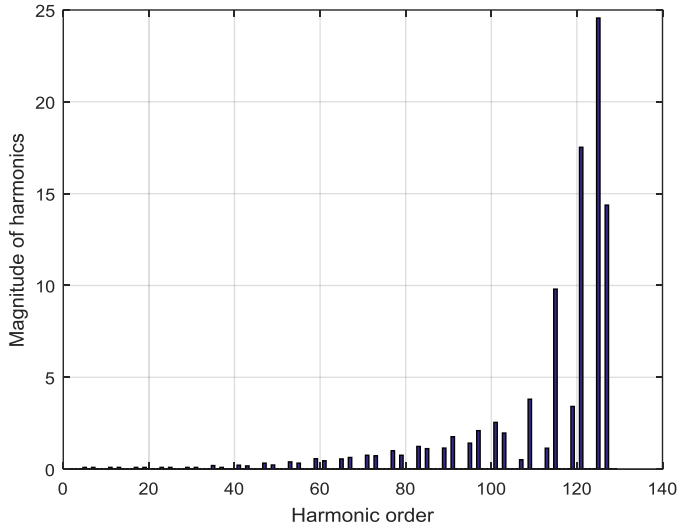


Figure 7. Harmonics distribution of V_{sn} with 60° DPWM.

5. Proposed Modulation Scheme

In the conventional DPWM switching method, many harmonic voltages are generated at the output terminal of the inverter due to the discontinuous variation of the modulation signal. This paper introduces new offset voltage V_{new_offset} by using the sixth harmonic injection technique to V_{offset} in order to reduce the harmonic voltages, as shown in Figure 8. The offset voltage of 60° DPWM is changed every 60° and the period of sixth harmonic is same as that of 60°. In the range where the sixth harmonic is injected, sixth harmonic can be easily injected because the direction of change of sixth harmonics and the offset voltage is same. In proposed method, the clamping range of the modulation signals is reduced 30° from 60°. In the case that the maximum value of V^*_{xs} is positive, V_{new_offset} is changed depending on the sixth harmonic during the first and the last 15° range in the clamping range. In the other range, V_{new_offset} can be obtained in the same manner of the 60° DPWM. In the opposite case, V_{new_offset} can be obtained in the same way, as descripted above. To inject proper sixth harmonic, it is necessary to optimize the amplitude of the sixth harmonics. A half period of V_{offset} is same as the period of the sixth harmonic because the frequency of the sixth harmonic is twice than that of V_{offset}. When considering the unit sixth harmonic that the magnitude is 1, the magnitude of the sixth harmonic is 1 at the point the sixth harmonic injection is completed during the first 15° range. In the same way, at the point the sixth harmonic injection begins during last 15° range, the magnitude of the sixth harmonic is -1. Therefore, to inject the proper sixth harmonic at the second point mentioned above, the magnitude of the sixth harmonic and V_{offset} should be same. Therefore, the proposed method uses V_{offset} to the magnitude of the sixth harmonic. If V_{offset} is used in the magnitude of the sixth harmonic, the optimized sixth harmonic can be injected to V_{offset}.

Figure 9 shows the modulation signal of the proposed algorithm. V^*_{xn} is the sum of V^*_{xs} and V_{new_offset}, like Equation (5) for conventional DPWM. V^*_{xn} is expressed as

$$V^*_{xn} = V^*_{xs} + V_{new\_offset} \tag{17}$$

In the proposed DPWM switching method, V_{new_offset} varies smoothly by injecting the sixth harmonics to V_{offset} unlike the conventional DPWM and the modulation signal is softly clamped to the DC-bus, as illustrated in Figure 9. Therefore, when using the proposed switching method, many harmonics of the output voltage of the inverter can be reduced.

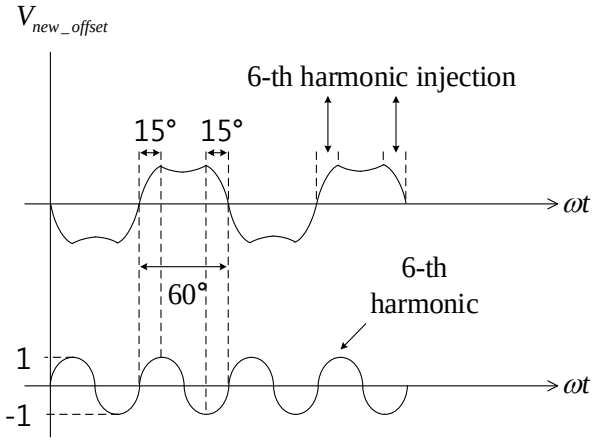


Figure 8. Injection of the sixth harmonic component to the offset voltage.

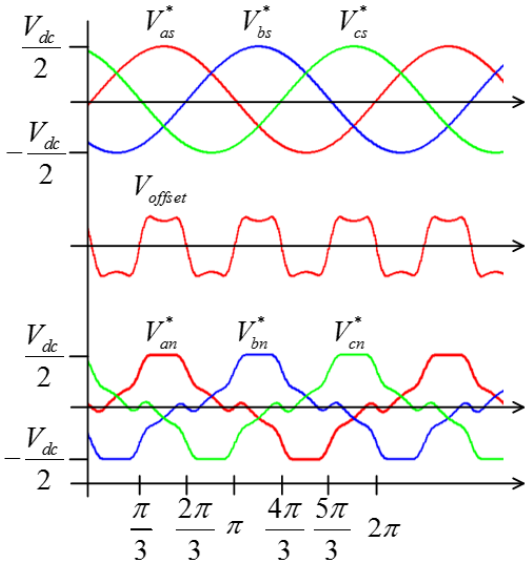


Figure 9. Voltage modulation signal of the proposed DPWM.

Figure 10 shows the harmonics distribution of V_{sn} with the proposed DPWM under the same conditions, as in Figure 7. N = 1 and 129 harmonics are excluded from Figure 10, and y-axis scale is the same with that of Figure 7, which allows to see the lower order harmonics in detail. When the proposed DPWM is implemented to the switching method, the harmonics of the switching frequency band have the greatest magnitude. It is similar to the results, as shown in Figure 7. However, the distribution of the lower order harmonics is different from that of Figure 7. In Figure 10, the harmonics below N = 100 are reduced and are not distributed in a wide frequency range when compared with that of Figure 7. Therefore, the lower order harmonics that are less than the half of the switching frequency are also reduced. If the harmonic voltages overlap the resonance frequency band caused by the LCL-filter, the problem of the resonance current does not occur because the harmonic voltages in the resonance frequency band are sufficiently reduced. Consequently, the grid current does not oscillate every 60° when the modulation signal is clamped to the DC-bus.

The proposed method uses sixth harmonic injection technique to reduce the resonance current. When using this method, the quality of the grid current is improved because the resonance components of the grid current can be sufficiently reduced. However, the proposed DPWM has a disadvantage regarding the efficacy because the clamping range is too narrow to inject sixth harmonics to V_{offset}.

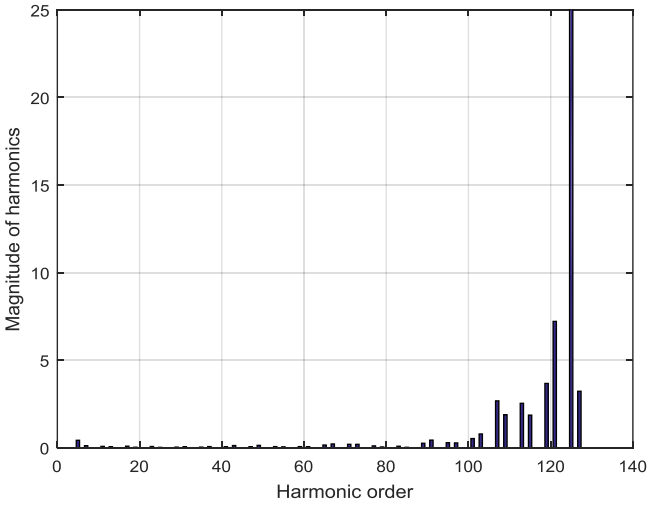


Figure 10. Harmonics distribution of V_{sn} with the proposed DPWM.

Figure 11 shows switching states of three-level inverter with the proposed DPWM (T_1, T_2, T_3, and T_4 are shown in Figure 1). If the a-phase reference voltage is positive, it is compared with the upper carrier signal and T_1, T_3 are triggered. T_1 and T_3 operate complementarily. T_2 and T_4 maintains ON and OFF state. In the opposite case, the reference voltage is compared with lower carrier signal and T_2, T_4 are triggered. T_2 and T_4 also operate complementarily. T_3 and T_1 maintains ON and OFF state. The switches of b- and c-phase are triggered in the same way, according to the reference voltage.

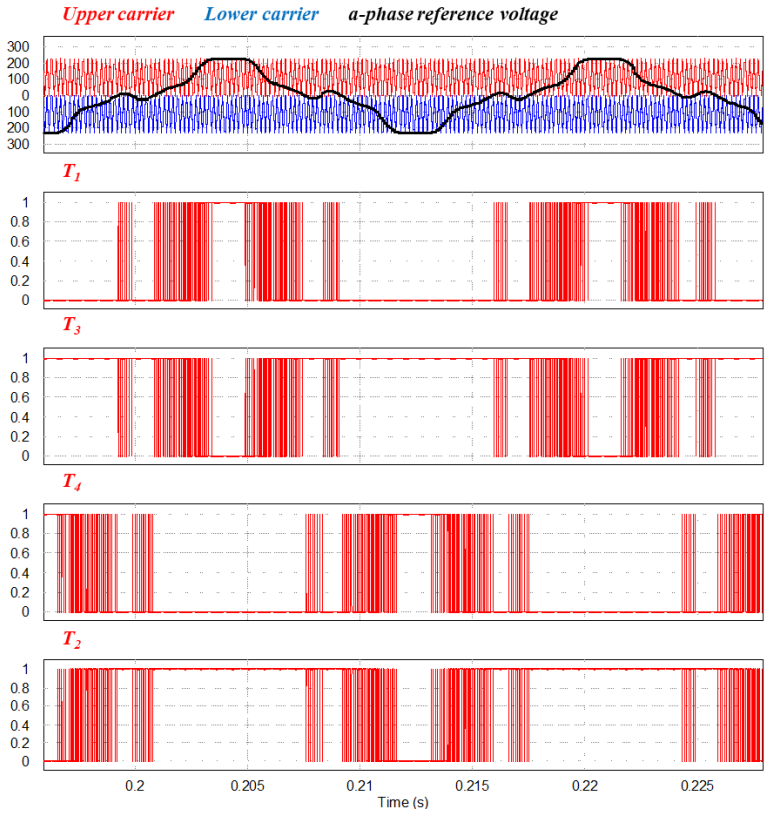


Figure 11. Switching state of 3-level inverter with the proposed DPWM.

6. Simulation Results

To confirm the validity of the proposed algorithm, a simulation was performed using a Powersim (PSIM) simulation (Powersim Inc., Rockville, MD, USA). The simulation circuit is the same as Figure 1. The simulation parameters are given in Table 1.

Table 1. Parameters for the simulation and the experiment.

Input Side		Output Side	
$V_{line\text{-}to\text{-}line}$	220 V_{ac} (rms)	DC-link voltage	450 V_{dc}
L_i	1.4 mH	DC-link capacitor	6800 μF
L_g	0.71 mH	Switching frequency	7.8 kHz
C_f	4.4 μF	-	-

Figure 12 shows V^*_{an}, V_{offset}, and the grid current of the conventional DPWM. V^*_{xn} is clamped to the DC-bus by V_{offset}.

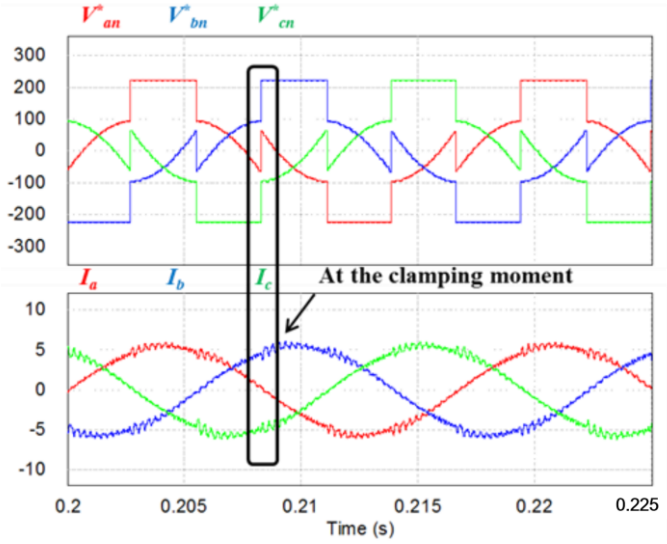


Figure 12. Modulation signal and grid current of the conventional DPWM.

V_{xs} has a number of harmonic voltages and these harmonics are generated at the moment when V^*_{xn} is clamped to the DC-bus. In the conventional DPWM switching method, the harmonic voltages are distributed in the wide frequency range. The harmonics also exist in the resonance frequency band. From Equation (1), $f_{resonance}$ is obtained as 3495 Hz by the LCL-filter and the resonance frequency band is formed around $f_{resonance}$. In the simulation condition, $f_{resonance}$ overlaps the harmonic voltages of V_{xs}. Therefore, the grid current oscillates at the moment that V^*_{xn} is clamped to the DC-bus every 60°, as shown in Figure 12.

Figure 13 shows the performance of the proposed algorithm. The system operates under the same condition, as in Figure 12. The proposed method injects the sixth harmonic to V_{offset} to reduce many harmonics of V_{xs}. V^*_{xn} is continuously clamped to the DC-bus as shown in Figure 13. It is possible to reduce many harmonics of V_{xs} because the discontinuous variation of V_{offset} disappears. $f_{resonace}$ is still 3495 Hz by the LCL-filter. However, the harmonic voltages are sufficiently reduced. In particular, the harmonics of the resonance frequency band also are reduced. Therefore, the grid current does not oscillate at the moment that V^*_{xn} is clamped to the DC-bus.

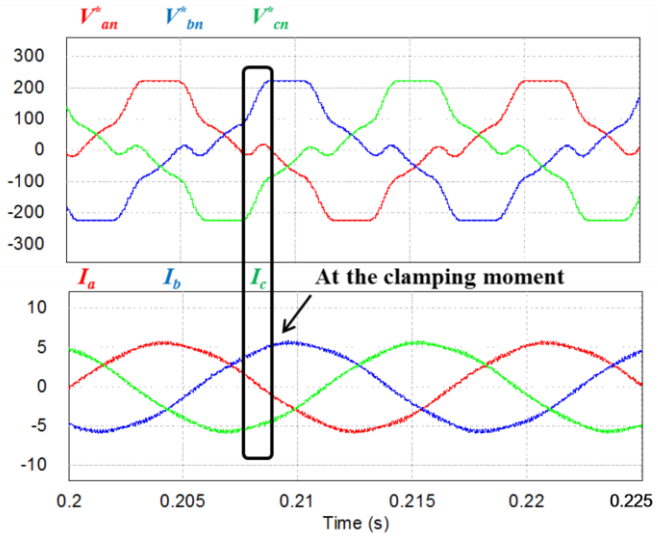


Figure 13. Reference voltage and grid current of the proposed DPWM.

7. Experimental Results

The Experiments were performed to verify the proposed method. Figure 14 shows the hardware setup. This set consists of a control board, a sensor board, gate drivers, and LUH50G1204 IGBT modules from LSIS (LS Industrial Systems Co., Ltd., Anyang-si, Korea). The experimental setup parameters are the same as the simulation parameters, as shown in Table 1.

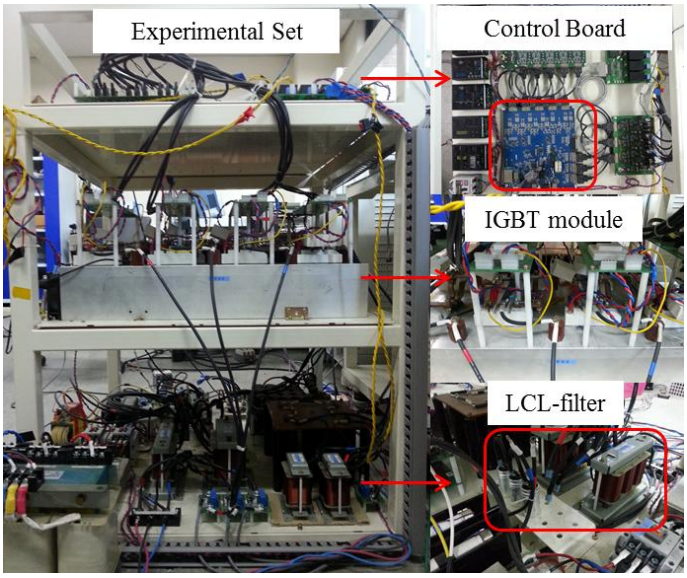


Figure 14. Experiment set of the neutral-point clamped (NPC)-type inverter.

Figure 15 shows the reference of the a-phase pole voltage V^*_{an}, V_{offset}, and the a-phase pole voltage V_{an} in the conventional DPWM. V_{offset} discontinuously changes every 60°. V^*_{an} is clamped to the DC-bus as the variation of V_{offset}. In accordance with V^*_{an}, V_{an} is also clamped to the DC-bus and V_{an} maintains the DC-link voltage in the clamping range because the switching device is not switched.

Figure 16 shows the V^*_{an}, V_{new_offset}, and V_{an} of the proposed DPWM. V_{new_offset} smoothly changes every 60° when compared with V_{offset}, as shown in Figure 14, because the proposed method injects the sixth harmonic to V_{offset}. This method can soften the variation of V^*_{an} when V^*_{an} is clamped to the DC-bus. In the proposed algorithm, the clamping range is too narrow when compared with that of the

conventional DPWM due to the range where the 6-th harmonic is injected. For the reasons described above, the range in which V_{an} maintains the DC-link voltage is narrow compared with Figure 15.

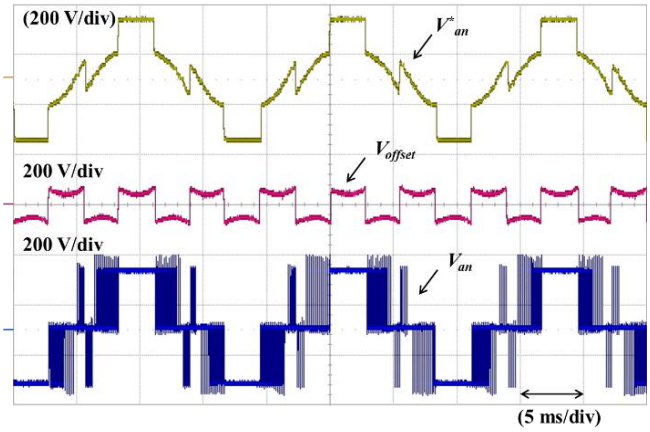


Figure 15. Modulation signal and pole voltage of the conventional DPWM.

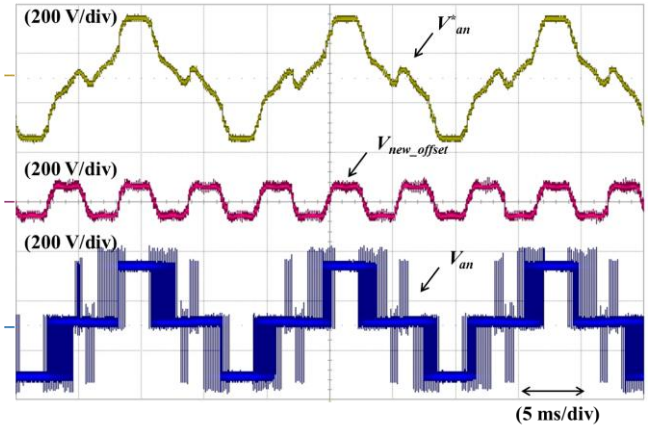


Figure 16. Modulation signal and pole voltage of the proposed DPWM.

Figure 17 shows the V^*_{an} and the a-phase grid current I_a in the conventional DPWM. V_{as} has many harmonic components, which are generated at the clamping moment where V^*_{an} is discontinuously changed. When these harmonic frequencies overlap $f_{resonance}$, the resonance problem of the grid current occurs. Figure 17a shows the resonance problem of the grid current. As mentioned above, I_a oscillates at the clamping moments, as shown in Figure 17a. When using the conventional DPWM, the efficiency of the system is improved because the switching devices are not switched in the clamping range. However, the resonance of the grid current causes the problem that adversely affects the quality of the grid current. Figure 17b shows the harmonics of I_a in the frequency domain. I_a has many harmonics, particularly in the resonance frequency band. The magnitude of the resonance components of I_a is approximately 0.2 A, as shown in Figure 17b.

Figure 18 shows the performance of the proposed DPWM. Unlike V^*_{an} shown in Figure 17a, V^*_{an} continuously changes, as shown in Figure 18a. Many harmonics of V_{as} are reduced because the sixth harmonic injection technique smoothly modifies V^*_{an}. Therefore, I_a does not oscillate at the clamping moment, as shown in Figure 18a. Figure 18b shows I_a in the frequency domain. When comparing with the result of Figure 17b, many harmonics of I_a in the resonance frequency band are sufficiently reduced. The magnitude of the resonance component of I_a is approximately 0.04 A, as shown in Figure 18b.

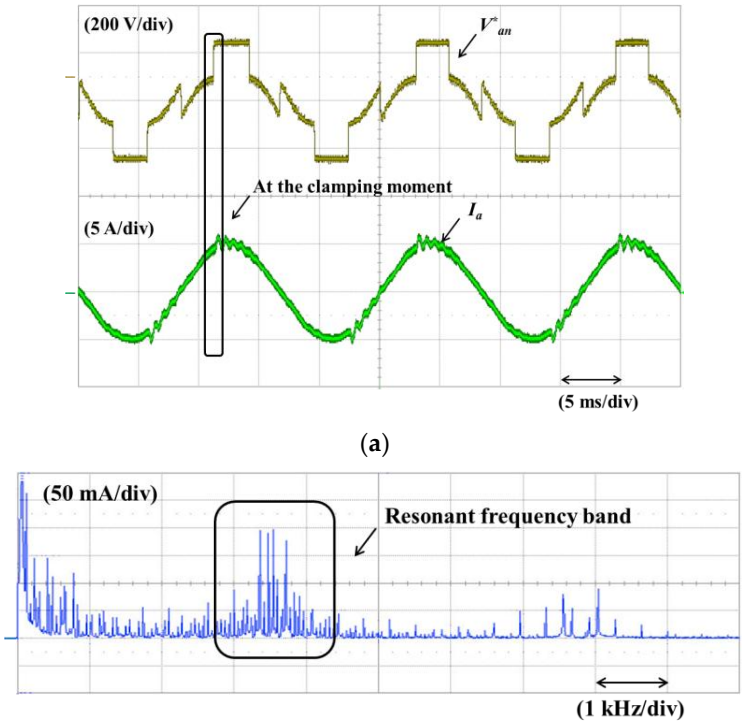


Figure 17. Modulation signal and the grid current with the conventional DPWM. (**a**) Modulation signal and grid current in the time domain; (**b**) grid current in the frequency domain.

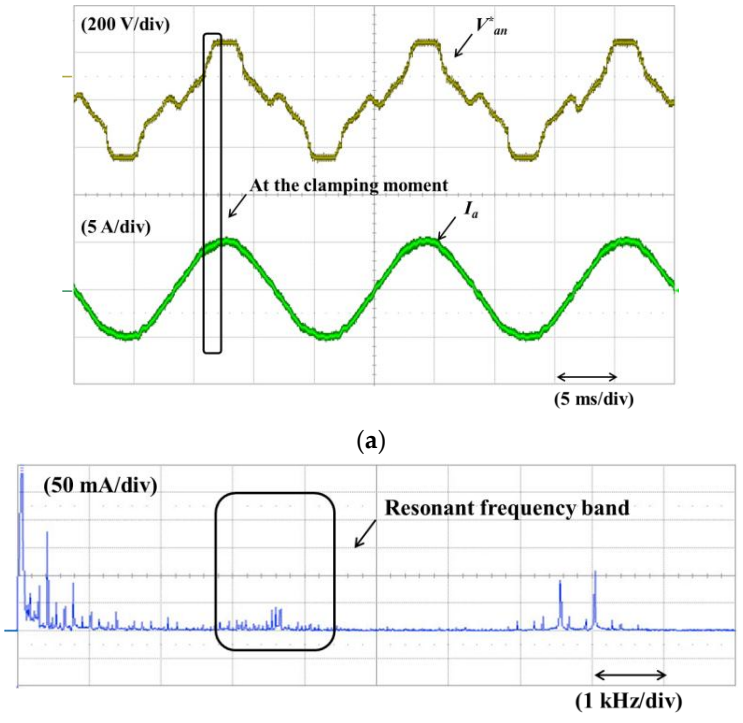
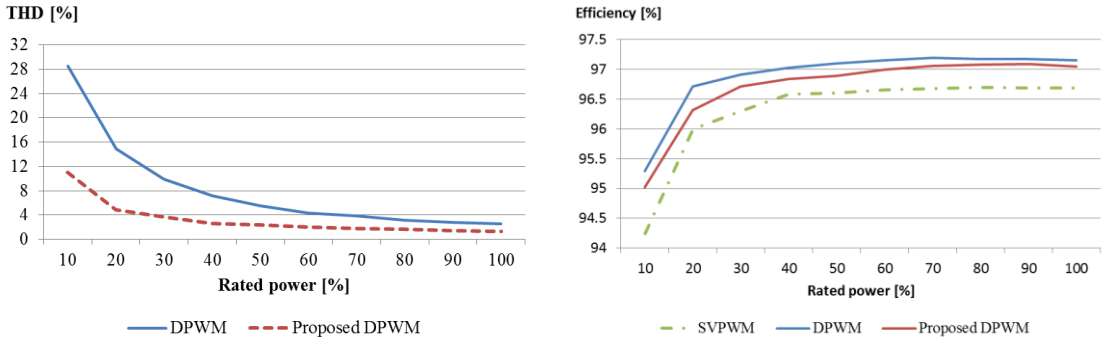


Figure 18. Modulation signal and the grid current with the proposed DPWM. (**a**) Modulation signal and grid current in the time domain; (**b**) grid current in the frequency domain.

Figure 19 compares the efficiency and the THD of the grid current, according to the switching methods. The THD and the efficiency were measured using the WT3000 power analyzer (YOKOGAWA, Tokyo, Japan). In Figure 19a, the THD of the conventional DPWM and the proposed DPWM are compared according to the loads. In the conventional DPWM, the grid current has the resonant components, which adversely affect the THD. However, the proposed DPWM improves the THD when compared with that of the conventional DPWM because the proposed DPWM can reduce the resonance current. Figure 19a shows the result that the THD of the proposed DPWM is lower than that of the conventional DPWM for the entire load range. Figure 19b shows the efficiency of three modulation signals: SPWM, the conventional DPWM, and the proposed DPWM. The conventional DPWM and the proposed DPWM have the advantage of the lower switching loss because both methods have a clamping range where the switching devices are not operated. Therefore, the efficiency of both modulation methods is 1% higher than that of the SPWM. When comparing the conventional DPWM and the proposed DPWM, the clamping range of the proposed DPWM is narrower than that of the conventional DPWM because the proposed DPWM has the region where the sixth harmonic is injected. For this reason, the efficiency of the proposed DPWM is slightly lower than that of the conventional DPWM because the switching loss of the proposed DPWM is higher than that of the conventional DPWM.



(**a**) (**b**)

Figure 19. Performance of the proposed DPWM according to MI. (**a**) Total harmonic distortion (THD) of the grid current; (**b**) Efficiency.

8. Conclusions

This paper proposed the DPWM method to solve the resonance problem in a grid-connected inverter system using the LCL-filter. The Modulation signal of the 60° DPWM is discontinuously changed and many harmonic voltages are generated in the wide frequency range at the output terminal of the inverter. The grid current has the resonance component because these harmonic voltages are present in the resonance frequency band. The modulation signal of the proposed DPWM is continuously changed by injecting the sixth harmonic to the modulation signal, and a number of harmonic voltages can be reduced. The proposed DPWM solves the resonance problem by the sufficient reduction of the harmonic voltages in the resonance frequency band. The effectiveness and the performance of the proposed DPWM for a grid-connected inverter system using the LCL-filter were verified by the simulation and the experiment.

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Conflicts of Interest: The authors declare no conflict of interest.

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