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# A Stable and Fast-Transient Performance Switched-Mode Power Amplifier for a Power Hardware in the Loop (PHIL) System

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**Abstract:** Power Hardware in the Loop (PHIL) systems are used to test a power system with the help of combined software and hardware. Generally, to construct a PHIL system, a switched-mode power amplifier that has a stable performance is used, because of their large, linear signal control-to-output characteristics. However, the fundamental limitations of a switch-mode power amplifier (PA) are the dynamic performance and output bandwidth. In this paper, a compound controller has been used for the rectifier part of a PA, which can ensure the stability of a PA under transient or fault operating conditions. Moreover, a compound controller, which involves a feed-forward controller, a proportional controller and a repetitive controller, is proposed in the inverter part of a PA, and it can be used for PHIL applications. Experimental results are obtained under various operating conditions, such as transient responses under load step change, and output voltage bandwidth testing for a PHIL system, it is concluded that a proposed switched-mode power amplifier is useful for the PHIL system.

**Keywords:** power hardware-in-the-loop; power amplifier; compound controller; dynamic performance

## 1. Introduction

Power Hardware in the Loop (PHIL) [1] is a real-time simulation technology that is widely used in power systems for facility testing and validation [2–6]. A general architecture of a PHIL system is shown in Figure 1.

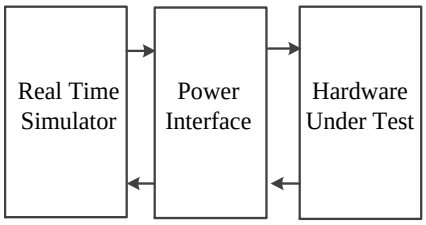


**Figure 1.** The basic building block of a Power Hardware in the Loop (PHIL) system.

There are three parts in PHIL system, one part is a real time simulator (RTS) [7], another one is the hardware under test (HUT) [8], and the power interface (PI) [9] is a system connected between the other two parts. In a PHIL system, the reference signal is obtained from the RTS part, and it is applied to the terminals of the HUT through the PI to establish a virtual exchange of power between the RTS and HUT. The signals are high-powered. Many PHIL simulations are used, for example, the HUT

parts involved can be distributed generation systems [10–12], electrical vehicles [13,14] and power grids [15–17]. A PHIL system is an attractive option for testing electrical equipment as it combines the benefits of digital simulation and laboratory testing. Moreover, it offers some important benefits [18], such as realistic conditions, flexibility, scalability, and derisking of equipment.

A PI is a key component of a PHIL system, and a power amplifier (PA) [19,20] is the main component of the PI part. Ideally, a PA should have an infinite bandwidth, unity gain, and zero time delay. However, this is neither achievable nor affordable. Generally, a switch-mode power converter [21,22], which tracks the reference signal accurately is used as PA, because of their inherent linear control-to-output characteristics. However, the dynamic performance and the output bandwidth of a switch-mode PA are the fundamental limitation. Thus, a PHIL system requires that a PA can operate stably, and have a better output bandwidth. Moreover, a very high output bandwidth is required while simulating transient or fault behavior in a power grid under different operating conditions.

To overcome the aforementioned limitations of a switch-mode PA, a back-to-back converter is proposed in this paper for PHIL applications [23]. The conventional controller of a PA has already been discussed in [24], but this was still unable to meet the PHIL simulation requirements. Therefore, a compound controller has been used for the rectifier part of a PA, which can ensure the stability of a PA under transient or fault operating conditions. Moreover, a compound controller, which involves a feed-forward controller, a proportional controller and a repetitive controller, is proposed in the inverter part of a PA. The proposed compound controller can be used for the PHIL applications.

A repetitive controller originating from the internal model principle [25,26] is known as an effective solution for rejection of periodic errors in a dynamic system. The core mechanism of this technique is to incorporate a modified internal model by properly constructing feedback loops of one or a few time delay units. Consequently, periodic errors can be eliminated. A number of repetitive controllers have been developed for inverters [27]. The conventional repetitive controller structure is based on a time delay, thus, it is proposed a compound controller to improve the PA simulation performance in this paper.

The general overview and details of various system components such as a real-time simulator, an interface algorithm, and interface card, etc., to build a PHIL simulator are given in Section 2. A math model of PA has been set up in Section 3. The compound controller for the rectifier part of a PA is described in Section 4. A compound controller for the inverter part of a PA is given in Section 5. The experimental results to prove the validity of the built PHIL platform using the proposed amplifier are given in Section 5 under various operating conditions and for different HUT power devices. The conclusions are given in Section 6, followed by references.

## 2. Overview of a PHIL System

An architecture of a PHIL system is given in Figure 2. The PHIL system is used for simulating a power grid, which is divided into two parts. One part is modeled on a real-time simulator, and the other part is set up in the power HUT. The key constituents of a PHIL system are described in the following subsections.

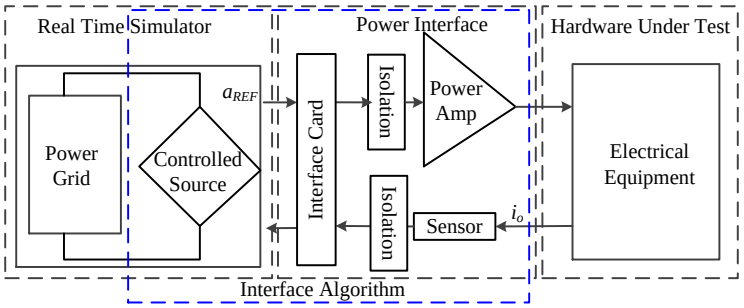


**Figure 2.** The architecture of a PHIL system.

### 2.1. Real-Time Simulator

As discussed earlier, the virtual network of the simulated power system is modeled and calculated in a real-time simulator (RTS), which is based on a computer program. Moreover, to achieve a better simulation accuracy, the sampling frequency should be much higher than the simulation frequency. Meanwhile, to deal with the simulation dynamic procedure, the simulation time steps should be low enough.

### 2.2. Power Interface

A power interface (PI) is a critical part of a PHIL system, which contains a power amplifier, interface card, sensor, and isolation. Figure 2 shows that a reference signal ($a_{REF}$) is obtained on the RTS side, and it is applied to the terminals of the actual hardware through the PI to establish a virtual exchange of power between the simulated virtual network and the power HUT. The PA is the main part of the PI, which elevates the power level of the signal coming from the RTS to a power level required by the HUT. The signals between the RTS and hardware are exchanged by the interface card. The sensor is used to sense the output current ($i_o$), which requires a high bandwidth. The RTS and HUT have been kept isolated.

### 2.3. Interface Algorithm

An interface algorithm is needed to connect the virtually simulated network and the physical hardware. Figure 3 shows the ideal transformer model (ITM) interface algorithm proposed in [18]. There are two types that are used in a PHIL system. One is controlled current source (CCS), which is arranged in the RTS. The other is controlled voltage source (CVS) inside the RTS. The ITM interface algorithm is a simple, accurate and efficient method, which is widely used in a PHIL system. In Figure 3a, the CCS is inside the RTS, and the power amplifier is used as a CVS. The reference signal ($u_1$) inside the simulator acts as a reference to the power amplifier ($u_2$), and the output current ($i_2$) act as a reference for the CCS ($i_1$) inside the RTS. Furthermore, the ITM interfacing algorithm can be also realized in a reverse arrangement of the controlled voltage or current source, as given in Figure 3b.

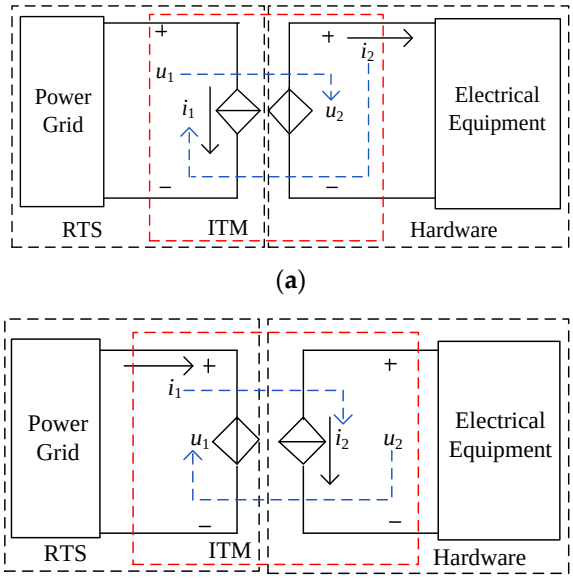


**Figure 3.** Ideal transformer model (ITM) interface algorithm (**a**) controlled current source (CCS) inside real time simulator (RTS); (**b**) controlled voltage source (CVS) inside RTS.

### 2.4. Power Amplifier in a PHIL System

A power amplifier is the main part of a power interface; moreover, it is an important element of the PHIL system. It converts the low-power signal coming from the RTS to high-power signals for HUT. The typical circuit structure of a single phase switch-type power amplifier is shown in Figure 4.

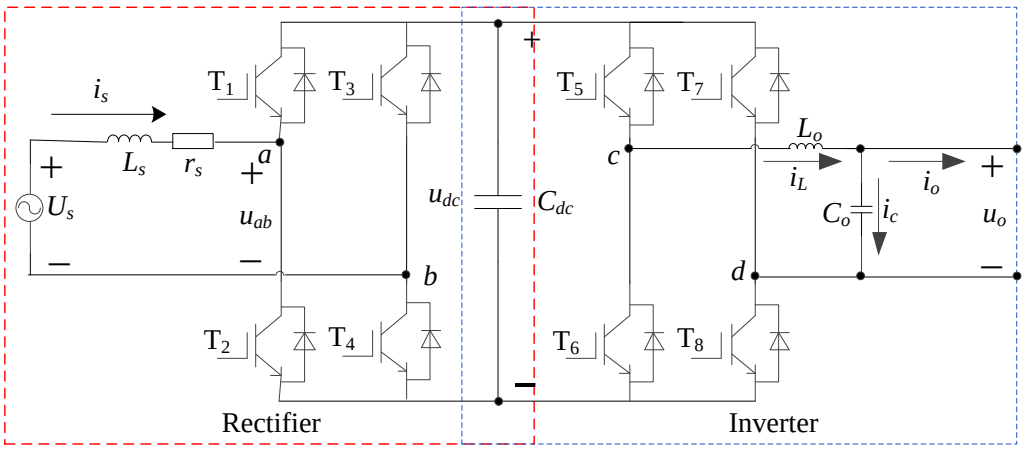


**Figure 4.** A typical circuit of single-phase power amplifier (PA).

This section describes the stat-space rectifier model and inverter model separately. To design a compound controller for a PA, a developed model is used to study the controller performance for the output bandwidth meanwhile ensuring the stability and a good dynamic response for all kinds of HUT. The model is developed based on the circuit schematic, given in Figure 4, which shows an insulated gate bipolar transistor (IGBT) (T1~T8)-based on back-to-back converter.

A grid voltage source $U_s$ is placed in series with a grid resistor $r_s$ and grid inductor $L_s$ in the rectifier part. Meanwhile, an averaged model with the modulation ratio $m_r$ is obtained:

$$\frac{d}{dt}\begin{bmatrix} i_s \\ u_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{r_s}{L_s} \\ -\frac{1}{R_o} \end{bmatrix}\begin{bmatrix} i_s \\ u_{dc} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L_s} \\ \frac{1}{C_{dc}} \end{bmatrix}\begin{bmatrix} m_r u_{dc} \\ m_r i_s \end{bmatrix} + \begin{bmatrix} \frac{U_s}{L_s} \\ 0 \end{bmatrix}, \tag{1}$$

In an inverter part, an output filter (inductor $L_o$, capacitor $C_o$) is used to suppress high-frequency switching components to prevent them from entering the HUT. The output voltage $u_o$ and the output current $i_o$ are imposed on the HUT part. In addition, the moving average of the switching functions are involved, which includes the modulation ratio $m_i$ and the bus voltage $U_{dc}$. The modulation ratio $m_i$ is equal to the peak of the control signal $U_r$ divided by the peak of the triangular carrier waveform $V_{tri}$. Although the parameter $V_{tri}$ is always constant, $u_{dc}$ may change depending on the grid conditions. It is relatively constant when the grid is correct due to the controlled rectifier. Therefore, the voltage $u_o$ and current $i_o$ equations can be written as follows:

$$\frac{d}{dt}\begin{bmatrix} u_o \\ i_L \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{C_o} \\ -\frac{1}{L_o} & -\frac{r_l}{L_o} \end{bmatrix}\begin{bmatrix} u_o \\ i_L \end{bmatrix} + \begin{bmatrix} 0 & -\frac{1}{C_o} \\ \frac{1}{L_o} & 0 \end{bmatrix}\begin{bmatrix} m_i u_{dc} \\ i_o \end{bmatrix}, \tag{2}$$

It is shown that the dynamic characteristics such as high bandwidth and fast response time, which determine the simulation performance of a PHIL system, are based on the inverter controller. Meanwhile, the rectifier part, which is under all kinds of disturbance on the dynamics of the DC bus voltage $u_{dc}$, is required to improve the rectifier controller.

## 3. Controller for the Rectifier of a PA

To design a controller for the rectifier part of a PA, a compound controller has been proposed:

(1) Controlling the DC side voltage, thus enabling the PA to be kept within the range required by normal operation;
(2) Guaranteeing the power quality on the DC side and avoiding the effect of a test on the conventional power grid. Thus, the objective of control of the rectifier side of the power interface is consistent with the objective of the control of the rectifier.

The block diagram of a double-loop controller of a power interface rectifier side is shown in Figure 5. $U_s$ is the grid-side system voltage. $u_{dcref}$ is the direct command voltage. $G_u(s)$ is the voltage controller. The main control objective of the outer voltage loop controller is to guarantee the static error of the system. Thus, a PI controller is used for the DC voltage with a scale coefficient of $k_{pz}$ and an integral coefficient of $k_{iz}$:

$$G_u(s) = k_{pz} + \frac{k_{iz}}{s}, \tag{3}$$

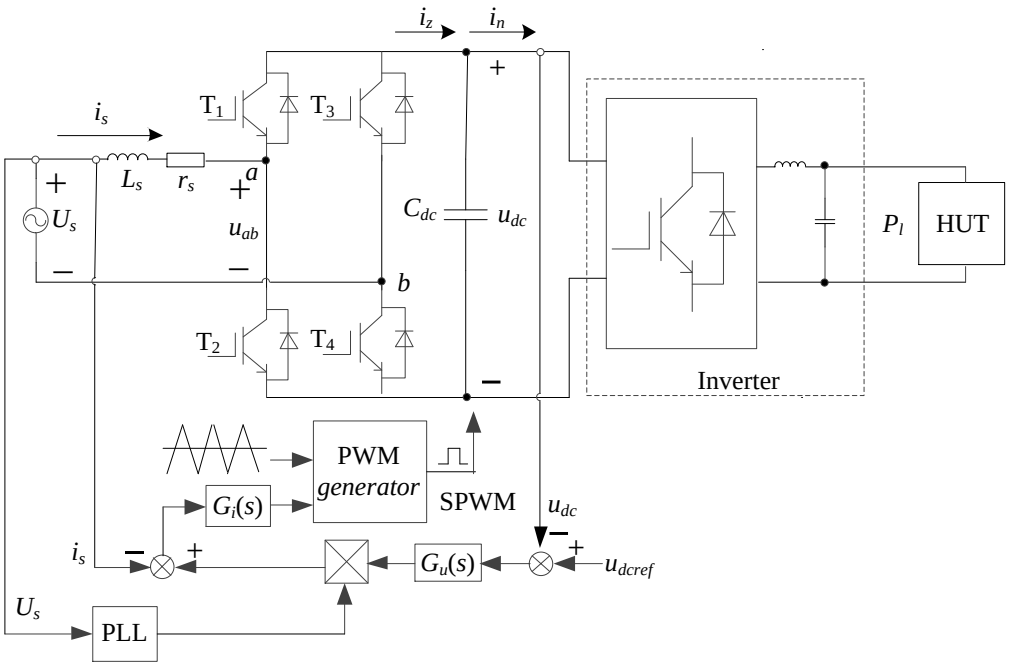


**Figure 5.** A proposed control scheme for a single-phase rectifier of a PA.

It is shown In Figure 6, a controller of a rectifier is proposed. $G_{inv}(s)$ is the equivalent inverter element. According to [28], a digitally controlled delay is considered which is equivalent to the first-order inertia element. $T_c$ is the switching cycle time. $K_{PWM}$ is the PWM bridge gain:

$$G_{inv}(s) = \frac{K_{PWM}}{0.5T_c s + 1}, \tag{4}$$

The controller of the current loop $G_i(s)$ mainly provides a fast tracking performance of a PHIL system. In this paper, single-loop control $k_{p1}$ is used to obtain the transfer function of the current loop:

$$G_{iz}(s) = \frac{k_{p1}K_{PWM}}{0.5T_c L_s s^2 + (L_s + 0.5T_c r_s)s + k_{p1}K_{PWM} + r_s}, \tag{5}$$

The binomial coefficient in Equation (5) is much smaller than the monomial coefficient when the switching frequency is high enough, and $T_c$ is small enough. The value of the internal inductor is very small relative to the proportional gain $k_{p1}$, hence, the second-order term can be ignored. Meanwhile, $T_i$ is the equivalent coefficient. Then the simplified equivalent element of the current loop can be obtained:

$$G_{iz}(s) \approx \frac{1}{1 + \frac{(0.5T_c r_s + L_s)}{k_{p1} K_{PWM}} s} = \frac{1}{1 + T_i s}, \tag{6}$$

Based on Equation (6) and Figure 6, the simplified outer voltage loop controller can be achieved as shown in Figure 7.

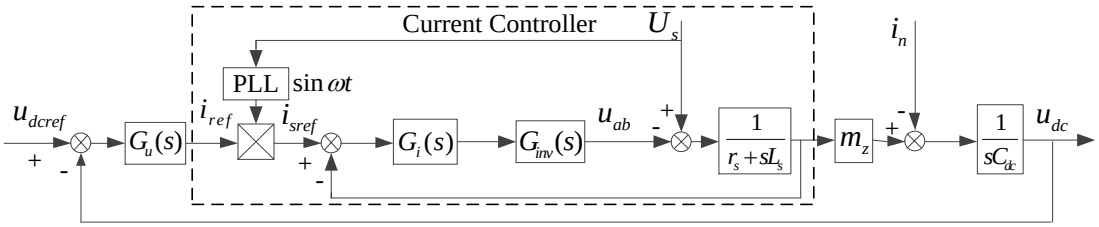


**Figure 6.** A proposed controller for the rectifier of a PA.

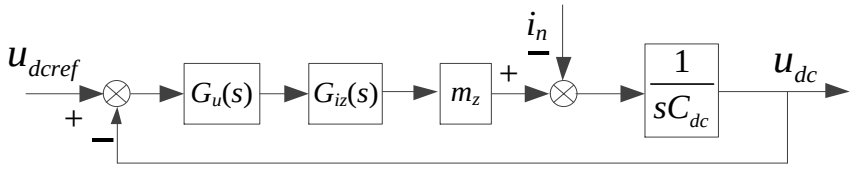


**Figure 7.** The equivalent for the rectifier of a PA.

### *3.1. The Dynamics Analysis of DC Bus Voltage under the Disturbance*

In a PHIL system, when the physical devices are connected to or disconnected from the system or the equipment power changes, it is difficult for the input power of the rectifier side to keep pace with the changes in load power due to the time lag that occurs in the controller of the PA. In particular, the dynamic response of a PI controller, which contain an outer voltage loop on the rectifier side, is slow. Meanwhile, the voltage of the DC bus fluctuates. Consequently, the disturbance transformation will lead to a voltage instability on a DC bus of the PA. It can even lead to system instable operate. Therefore, the stability and reliability of the PHIL system are greatly affected.

According to Figure 8, it is assumed that the arrowhead direction is positive, the active power on the DC side can be expressed as:

$$\begin{cases} P_i = u_{dc} i_z \\ P_o = u_{dc} i_n \end{cases}, \tag{7}$$

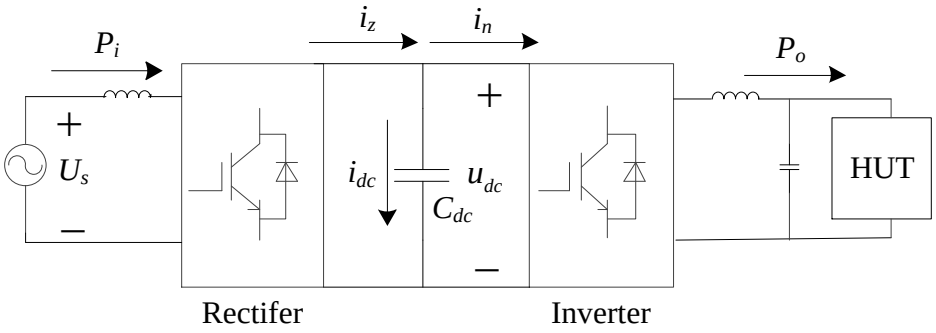


**Figure 8.** A typical circuit of single-phase power amplifier.

When the switching loss and a value of the inductor are ignored, $P_i$ can be expressed as the active power of the rectifier input and $P_o$ can be expressed as the load power. As shown in Figure 8, $u_{dc}$ is the voltage of the DC capacitor $C_{dc}$. $i_z$ is the current which flows into the DC capacitor and in is the efflux current of the DC capacitor. Thus, the capacitor current $i_{dc}$ can be expressed as:

$$i_{dc} = i_z - i_n = C_{dc}\frac{du_{dc}}{dt}, \tag{8}$$

Assuming that the power of the DC capacitor is $P_c$, according to the active power balance principle, the power balance equation for the DC side is:

$$P_c = P_i - P_o = u_{dc}i_{dc}, \tag{9}$$

Plugging Equation (8) into (9), it can be obtained that:

$$P_c = P_i - P_o = u_{dc}C_{dc}\frac{du_{dc}}{dt} = \frac{1}{2}C_{dc}\frac{du_{dc}^2}{dt}, \tag{10}$$

The capacitor voltage $u_{dc}$ would not suddenly change according to the circuit principle when the load power $P_o$ changes abruptly, according to the Equations (8) and (10) In this case, the change in load power is reflected by the change in the DC voltage, which is a disturbance quantity that influences the DC voltage, and it will lead to system instability.

### *3.2. A Current Feed-Forward Controller for the Rectifier of a PA*

According to the compensation principle in control theory [29], the feed-forward control introduces various disturbance inputs to compensate for their influence. Essentially, it is an open-loop control method. Thus, feed-forward control would not change the stability of the feedback system. From the perspective of disturbance suppression, the feed-forward control can share the burden on the controller. Therefore, the combination of the feed-forward control and the feedback control can improve the dynamic performance and maintain the stability of the system without increasing the open-loop gain. In order to analyze this conveniently, the average model of the state space is further linearized to obtain a small-signal model of the system, as shown in Figure 9.

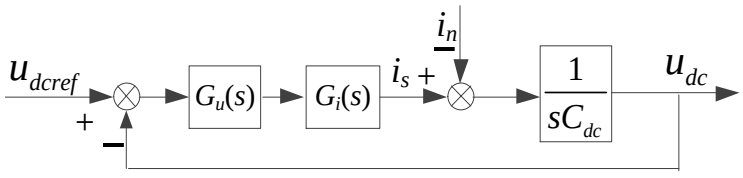


**Figure 9.** Block Diagram for Control of Direct Voltage.

Then, the transfer function $u_{dc}(s)$ of the DC capacitor voltage on the rectifier side of the power interface can be derived:

$$u_{dc}(s) = \frac{k_{pz}s + k_{iz}}{C_{dc}T_i s^3 + C_{dc}s^2 + k_{pz}s + k_{iz}} u_{dcref}(s) - \frac{T_i s^2 + 1}{C_{dc}T_i s^3 + C_{dc}s^2 + k_{pz}s + k_{iz}} i_n(s), \tag{11}$$

Based on (11), the expression of the output impedance transfer function $Z_o(s)$ on the rectifier side of the power interface is:

$$Z_o(s) = \frac{u_{dc}(s)}{i_n(s)} = \frac{T_i s^2 + 1}{C_{dc}T_i s^3 + C_{dc}s^2 + k_{pz}s + k_{iz}}, \tag{12}$$

To inhibit the fluctuation of the capacitor voltage under dynamic conditions, it can be concluded that the efflux flow current of the DC capacitor in is one of the key factors that influence the perturbation based on the previous analysis. Thus, on the basis of the control block diagram in Figure 9, a current feed-forward control is proposed for power interface with the current in as the feed-forward quantity. The control block diagram is shown in Figure 10. $G_q(s)$ is the feed-forward control.

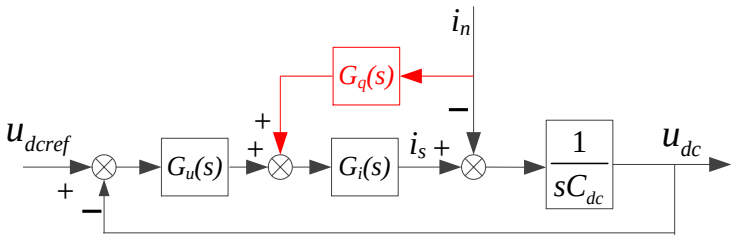


**Figure 10.** DC voltage control based on feed-forward control.

Based on Figure 10, the expression of the DC voltage of the feed-forward control with the current added in is:

$$u_{dc} = T_{ref}u_{dcref} - Z_{oz}i_n, \tag{13}$$

where, $T_{ref}$ is a disturbance quantity. The closed-loop transfer function $Z_{oq}$ of the system output impedance with disturbance quantity ignored can be expressed as:

$$Z_{oq} = \frac{u_{dc}}{i_n} = Z_o(1 - G_q G_i), \tag{14}$$

During the dynamic process of abrupt changes occurring in the measured equipment, the DC reference voltage $u_{dcref}$ and grid voltage $U_s$ on the rectifier side remain unchanged. Then the DC voltage fluctuation is only associated with the change in output current of the DC capacitor. According to (14), the DC voltage $u_{dc}$ fluctuates with the incoming disturbance. Ideally, in the case of $Z_{oq} = 0$, the effect of load disturbance on DC voltage can be completely eliminated. Then:

$$G_q(s) = G_i^{-1}(s) = \frac{0.5T_c L_s s^2 + (L_s + 0.5T_c r_s)s + k_{p1}K_{PWM} + r_s}{k_{p1}K_{PWM}}, \tag{15}$$

Based on Equation (15), the higher order terms can be ignored as the values of $T_c$ and $L_s$ are small. Approximate compensation is performed for the DC capacitor voltage disturbance of the power interface arising from abrupt changes in measured equipment. Then, we can obtain the expression of the feed-forward control:

$$G_q(s) = \frac{k_{p1}K_{PWM} + r_s}{k_{p1}K_{PWM}}, \tag{16}$$

To calculate the current feed-forward control coefficient of the rectifier side, we select the following conditions: grid impedance $L_s$ = 0.2 mH; loss impedance $r_s$ is equivalent to 0.5 Ω; DC bus capacitance $C_{dc}$ = 0.01 F; the inertia time constant $T_c$ = 200 μs; DC bus voltage on the rectifier side $U_{dc}$ = 400 V; the rated power of load is 16 kW; the outer loop control parameters $k_{pz}$ = 1, $k_{iz}$ = 100; current loop gain $k_{p1}$ = 0.7. Meanwhile, the gain is converted into the control parameters, i.e., inverter gain $K_{PWM}$ = 1. Finally, through the equivalent transformation, the current feed-forward control is approximately equivalent to a coefficient, i.e., $G_q(s)$ is equivalent to 1.5. Thus, we can obtain the frequency domain responses of output impedance transfer functions on the rectifier side with and without feed-forward control, $Z_o(s)$ and $Z_{oq}(s)$, as shown in Figure 11.

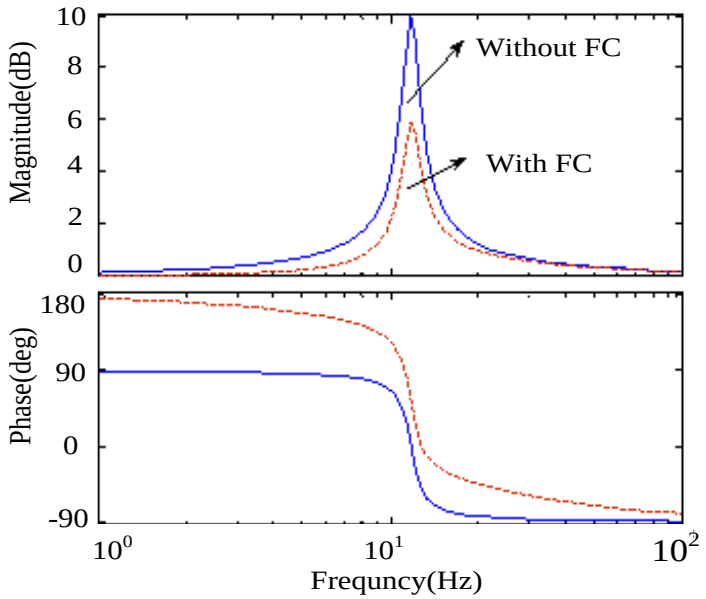


**Figure 11.** Characteristic curve for the output impedance frequency on the rectifier side of the power interface.

As seen in Figure 11, the resonance peak of the output impedance with feed-forward control (FC) decreases significantly compared with that without feed-forward control, and the former is almost half of the latter, which suggests that the feed-forward control can effectively inhibit the effect of the load current transformation arising from abrupt changes in measured equipment on the DC voltage. Thus, the anti-interference performance of the power interface is improved. However, because of a time delay in the sampling element, control computation, current control loop, etc., it is impossible for the current feed-forward control to completely eliminate disturbance, which is also consistent with the actual system.

## 4. Controller for the Inverter Part of a PA

This section presents the design of the proposed inverter controller. The architecture of an inverter of a PA is shown in Figure 12.

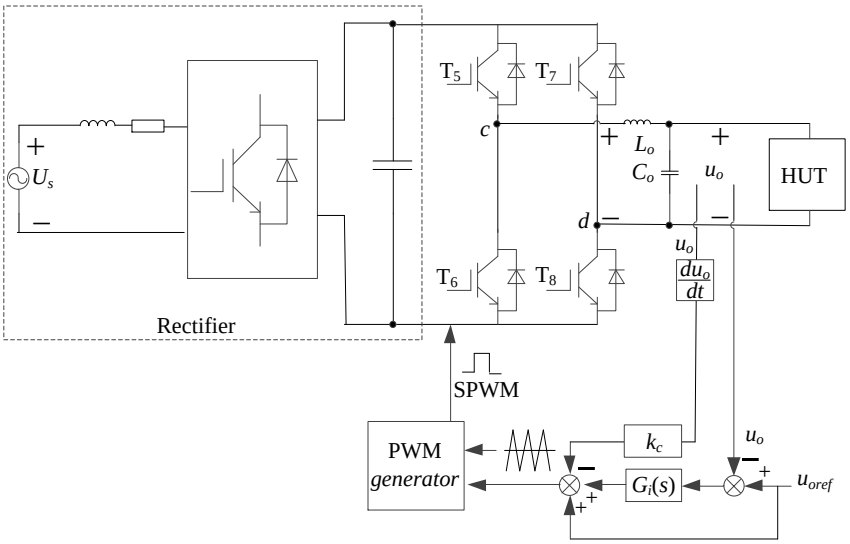


**Figure 12.** A proposed compound control scheme for a single-phase inverter of a PA.

### *4.1. Active Damping Compensator (ADC)*

An inverter system with a second-order LC filter commonly exhibits a sharp LC resonance peak, which leads to instability under no-load or light-load conditions. Therefore, either an inner current loop or an active damping loop will be helpful for stability compensation. According to [30], either inductor current or capacitor current feedback is valid for forming the current loop controller. However, they both need more current sensors, resulting in an increased total cost. Therefore, another approach is to utilize the capacitor voltage differential feedback [31]. It is easy to understand that the capacitor voltage differential is equivalent to the capacitor current without the high-resolution current sensors. Thus, this method will be used in the proposed control scheme.

The active damping factor kc is inserted in the LC transfer function. Then, the compensated LC filter transfer function and corresponding damping ratio can be derived:

$$G_{LC}(s) = \frac{1}{L_o C_o s^2 + k_c C_o s + 1}, \tag{17}$$

$$\xi = \frac{k_c}{2\sqrt{L_o C_o}}, \tag{18}$$

When $\xi = 0.07$, $k_c$ can be calculated by Equation (18). Based on the aforementioned analysis, the Bode plot of the *LC* filter is obtained, which is given in Figure 13. It can be realized that the sharp *LC* resonance peak is compensated for by ADC.

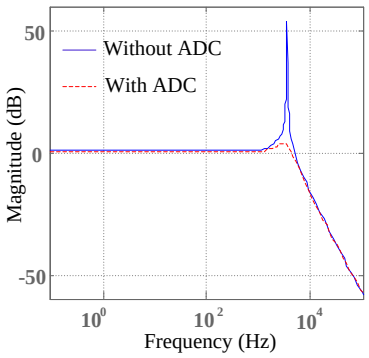


**Figure 13.** Bode plot of the LC filter transfer function.

### 4.2. Compound Controller

The discrete-time compound control scheme for a PA, which contains a repetitive controller and proportional controller, can be designed as shown in Figure 14. A reference feed-forward is incorporated to enhance the steady-state and dynamic performances. All the periodic disturbances are represented by $P(z)$. $u_{\text{ref}}(z)$ and $u_o(z)$ are the control reference and output voltage, respectively, $e(z)$ is the tracking error.

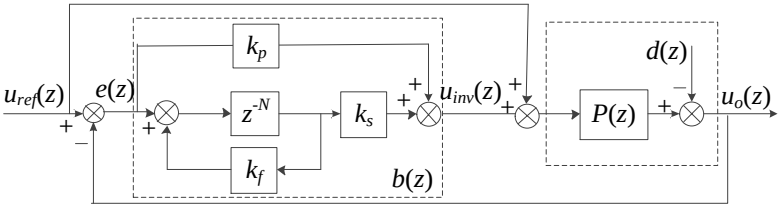


**Figure 14.** Discrete-time compound controller for a PA.

For simplification, here $b(z)$ represents the compound controller. $z^{-N}$ is the RC time delay unit. In practice, it occupies $N$ memory units for data storage in a digital implementation. Define $N$ as the number of samples in one fundamental period:

$$b(z) = \frac{u_{inv}(z)}{e(z)} = k_p + \frac{k_s z^{-N}}{1 - k_f z^{-N}}, \tag{19}$$

For simplification, the $P(z)$ and the disturbance $d(z)$ are obtained as (18), (19):

$$p(z)|_{z=e^{j\omega T_s}} = p(s)|_{z=j\omega} = \frac{1}{1 - C_o L_o \omega^2 + C_o r_l \omega j}, \tag{20}$$

$$d(z)|_{z=e^{j\omega T_s}} = d(s)|_{z=j\omega} = \frac{r_l + L_o \omega j}{1 - C_o L_o \omega^2 + C_o r_l \omega j} i_o(j\omega), \tag{21}$$

The transfer function of the reference $u_{ref}(z)$ can be represented by:

$$u_o(z) = \frac{p(z)b(z)}{1 + p(z)b(z)} u_{ref}(z) - \frac{1}{1 + p(z)b(z)} d(z), \tag{22}$$

Therefore, the Characteristic equation of transfer function is expressed as:

$$z^{-N} - k_f + \frac{k_s p(z)}{1 + k_p p(z)} = 0, \tag{23}$$

It can be found the general design criteria to meet the stability requirement, which is given by:

$$0 < k_s < (1 + k_f)(1 - C_o L_o \omega^2 + k_p), \tag{24}$$

According to [32,33] and from the aforementioned analysis, the theoretical upper limit of $k_r$ is 2, and $k_s$ is always 0.95. Moreover, it is noticeable that the $z^{-N}$ significantly affects the dynamic response of PA, hence, a proportional factor $k_p$ is proposed to enhance the dynamic response. However, an appropriate $k_p$ must be selected accordingly to meet the stability requirement. The proposed compound controller is implemented for a single-phase PA inverter.

To design an appropriate $k_p$, the design and analysis of the proposed controller have been done using the Simulink Control Design Linear Analysis tool which performs linearization and steady-state operating point analysis of a model built in the Simulink, and also generates various small-signal plots including bode, step response. Therefore, the magnitude and phase responses of the compound

controller when $k_p$ = 2, 5, 10 are illustrated in Figure 15, which shows that the bigger the value of $k_p$, the better the bandwidth that is obtained.

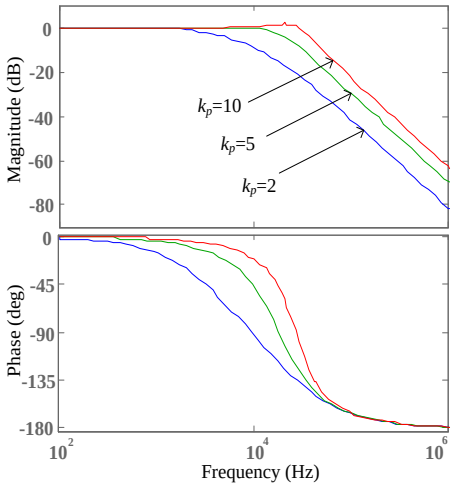


**Figure 15.** Discrete-time compound controller for a PA.

Moreover, the step response analysis of the closed-loop control system is obtained, as shown in Figure 16. When $k_p$ = 10, a fast-transient response is obtained. However, this results in a big overshoot, and can even affect the stability of the system. When $k_p$ = 2, it is expressed as a slow-transient performance. When $k_p$ = 5, it achieves a fast-transient response and stable performance.

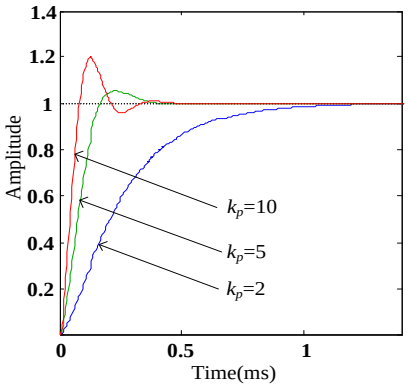


**Figure 16.** Discrete-time compound controller for a PA.

## 5. Experimental

To further verify the correctness of the theoretical analysis and simulation in this paper, an independent three-phase H-bridge back-to-back power interface and its controller are built based on the rectifier side and the inverter side in Figures 5 and 12. The structure of the test platform established is shown in Figure 17. The platform can operate in a single phase or in three phases.

In Figure 17, a voltage source Us, which is in series with internal impedance $Z_1$, and is capable of generating a fundamental and harmonic wave, is built in the Real Time Digital Simulator (RTDS). The interface model uses the ITM interface algorithm. $i_f$ is the feedback current of the measured equipment. $Z_i$ is the infinite internal impedance. The interface link outputs the voltage command signal $u_{ref}$ which controls the voltage output on the inverter side of the power interface to the measured equipment. In this section, the tested equipment is the power variable load $Z_2$, which is applied in DC capacitor voltage anti-disturbance analysis of the power interface and the hybrid simulation testing experiment of the output bandwidth and dynamic response.

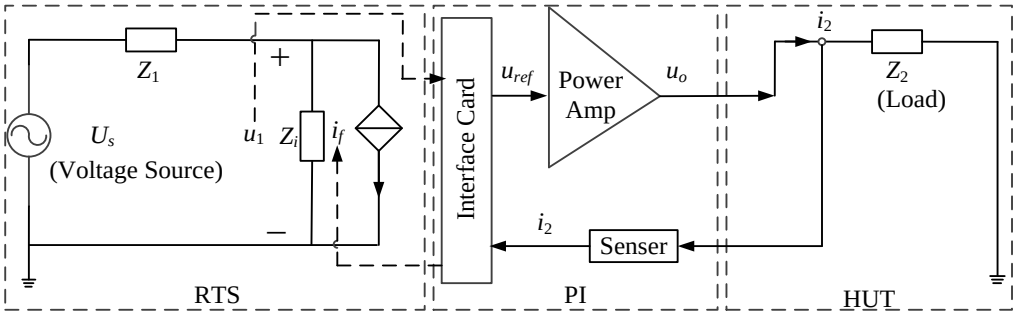


**Figure 17.** PHIL System.

The specific parameters and the simulation parameters are roughly the same. The grid voltage is 220 V. The DC bus voltage is 400 V. The switching elements for the power interface use the Infenone IGBT FF450R12ME4 (500 V/150 A). The switching frequency is 12.8 kHz. The controller core uses the ARM (STM32F417ZGT6) + FPGA (EP4C115F23I7N) chip.

### *5.1. DC Voltage Transient Responses Under Load Step Change*

Figures 18 and 19 show the control effects of abrupt power decrease and increase of power variable load. The waveforms shown are DC voltage $u_{dc}$, AC input current on the rectifier side of the power interface is $i_s$, and load current on the inverter side is $i_o$, respectively. Based on a comparison between Figure 18a,b, the DC voltage would rise excessively rapidly without feed-forward control when the system load declines abruptly. The voltage would be excessively high and the recovery time would also be long. The addition of feed-forward control inhibits the rapid rise and fluctuation of the DC voltage. Meanwhile, the voltage would become stable again in a short time. As shown in Figure 19a,b, when the load suddenly grows, the DC bus voltage with power feed-forward can rapidly recover to the command voltage, but the DC capacitor voltage without addition of the feed-forward control drops, leading to occurrence of protective action and causing the system operation to cease. Therefore, the experiment verifies the effectiveness and practicality of feed-forward control in inhibiting the DC capacitor voltage fluctuations caused by load disturbance and improving the system stability.

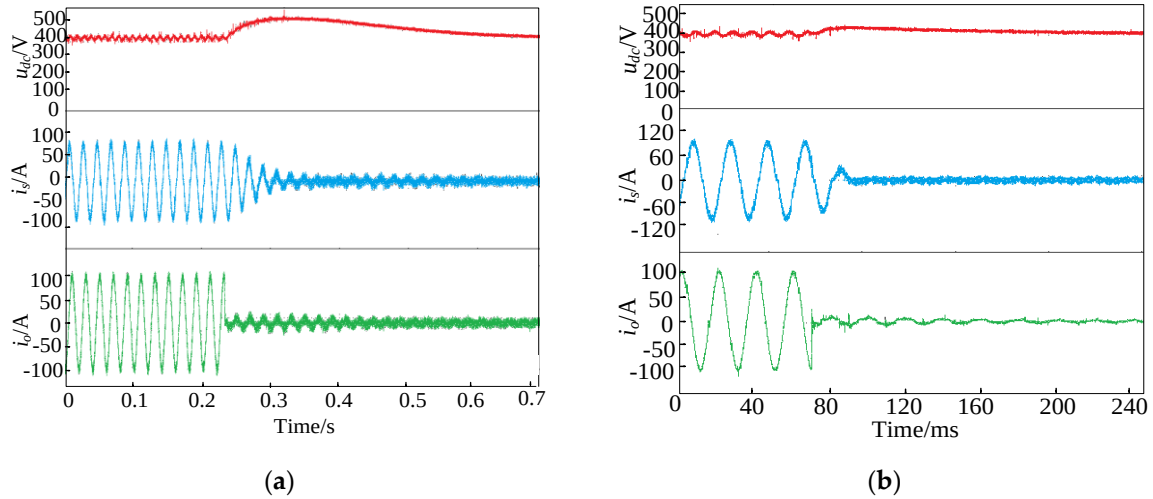


**Figure 18.** Comparison of Fluctuations of DC Capacitor Voltages in Two Control Methods in the Case of Abrupt Decline of Load Power. (**a**) Without addition of feed-forward control. (**b**) With addition of feed-forward control.

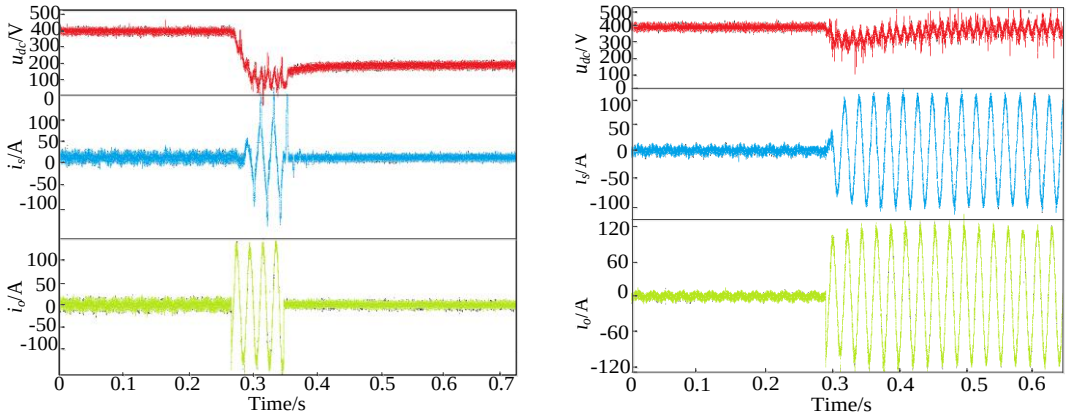


**Figure 19.** Comparison of Fluctuations of DC Capacitor Voltages in Two Control Methods in the Case of Abrupt Rise of Load Power. (**a**) Without addition of feed-forward control. (**b**) With addition of feed-forward control.

### *5.2. Waveform Analysis for the Dynamic Performance Test*

To further verify the effect of the controller proposed in this section on the dynamic performance of the power interface, a PHIL system is established on the basis of Figure 17 for testing. First, the voltage sources on the digital simulation side output voltages with fundamental wave and high-order harmonic respectively. Thus, as shown in Figures 20–23, the 3rd, 9th, 15th, and 20th harmonic voltage of 20% fundamental amplitude are added to the output fundamental wave of the power interface. Then, the voltage source on the digital simulation side outputs the mixed voltage of the fundamental wave and multiple high-order harmonics. Figure 24 shows the output voltage waveform, which is fundamental wave plus 3rd harmonic of 10% fundamental amplitude and 11th and 25th harmonics of 5% fundamental amplitude.

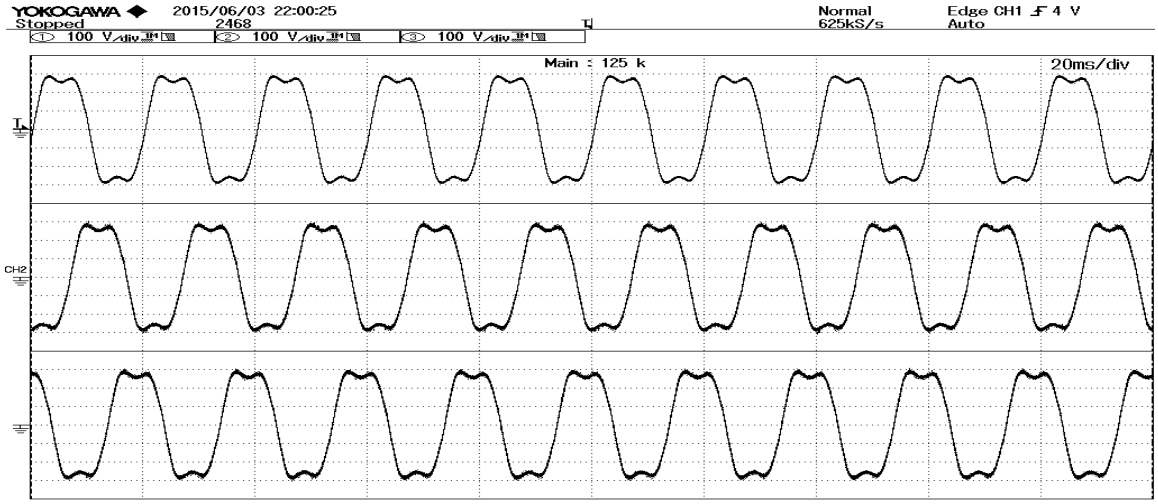


**Figure 20.** Fundamental wave + 3rd harmonic (20% fundamental wave amplitude) voltage waveform.

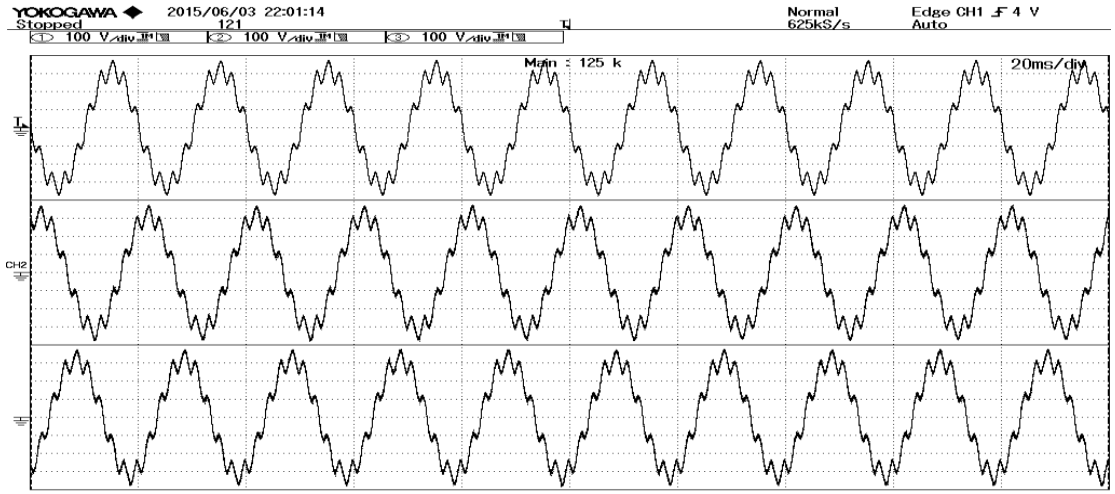


**Figure 21.** Fundamental wave + 9th harmonic (20% fundamental wave amplitude) voltage waveform.

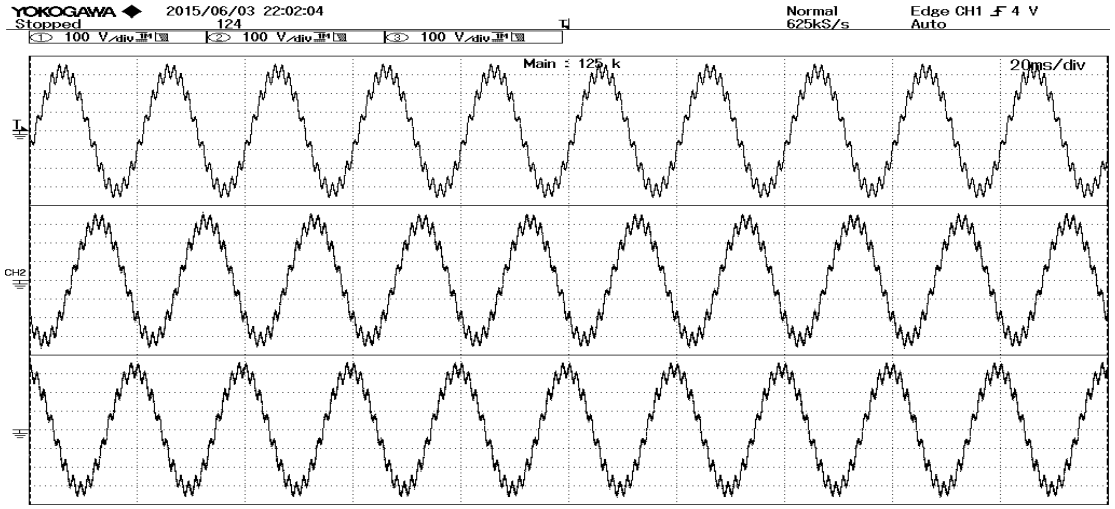


**Figure 22.** Fundamental wave + 15th harmonic (20% fundamental wave amplitude) voltage waveform.

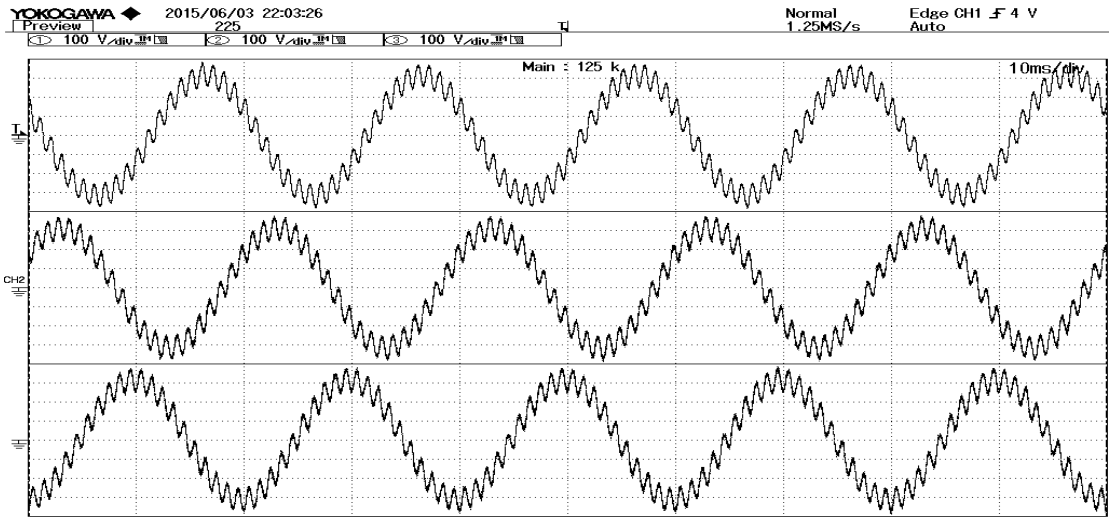


**Figure 23.** Fundamental wave + 20th harmonic (20% fundamental wave amplitude) voltage waveform.

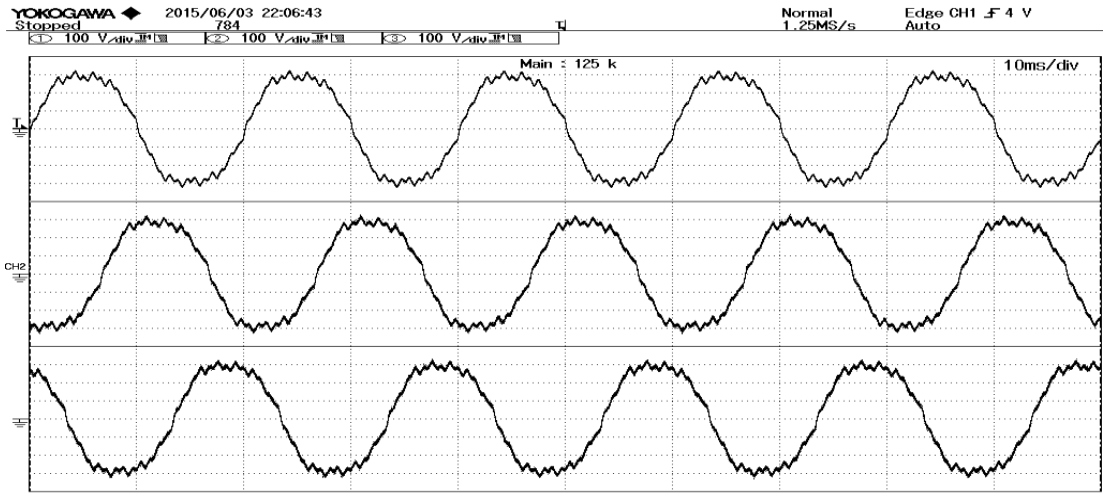


**Figure 24.** Fundamental wave + 3rd harmonic (10% fundamental wave amplitude) + 11th harmonic (5% fundamental wave amplitude) and 25th harmonic (5% fundamental wave amplitude) voltage waveform.

Figure 25 shows the output voltage waveform, which is the fundamental wave plus the 5th harmonic of 10% fundamental amplitude and the 15th and 23rd harmonics of 5% fundamental amplitude. Through the THD test equipment, this indicates that the output voltage waveform indeed contains the corresponding harmonics. Thus, it demonstrates that the power interface compound controller proposed in this paper can properly perform simulation amplification of the voltage harmonics and has excellent simulation bandwidth output.

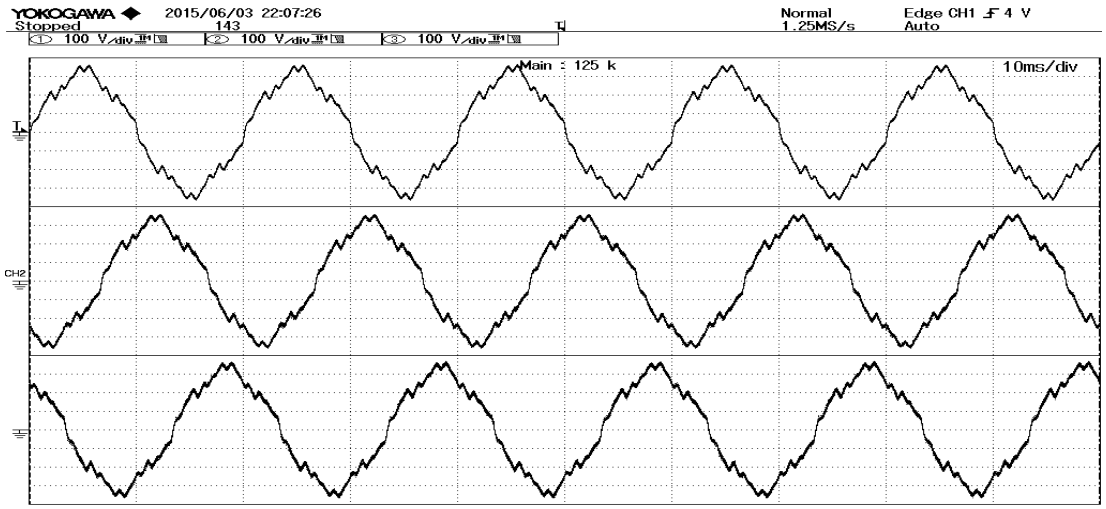


**Figure 25.** Fundamental wave + 5th harmonic (10% fundamental wave amplitude) + 15th harmonic (5% fundamental wave amplitude) and 23rd harmonic (5% fundamental wave amplitude) voltage waveform.

To further verify the simulation capacity of the power interface in the dynamic process of the system, a PHIL is designed on the basis of Figure 26 for testing. The power interface outputs stable three-phase fundamental voltage. At some point, a voltage sag of the voltage source on the digital simulation side occurs and then the hybrid simulation experiment is started. In Test 1, the voltage sag of the voltage source output is 70% and the state is maintained for 0.1 s. The dynamic process of voltage sag is as shown in Figure 26. In Test 2, the voltage sag of the power interface output is 100% and the state is maintained for 0.1 s. The dynamic process of voltage sag is shown in Figure 27. Through the waveform analysis, the transient process of the power interface output voltage designed in this section

lasts for approximately 0.3 s. Compared with the existing power interface in the literature, the power interface designed in this paper has better dynamic tracking performance. Thus, it is verified that the power interface based on the proposed compound controller has good dynamic performance.

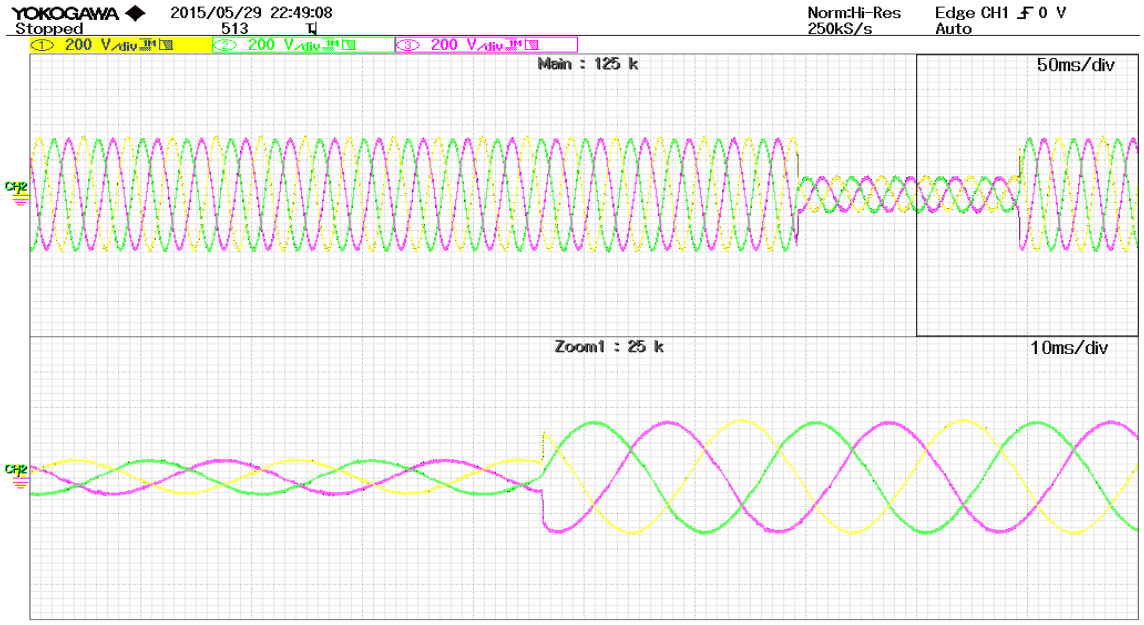


**Figure 26.** Output Voltage sag by 70%.

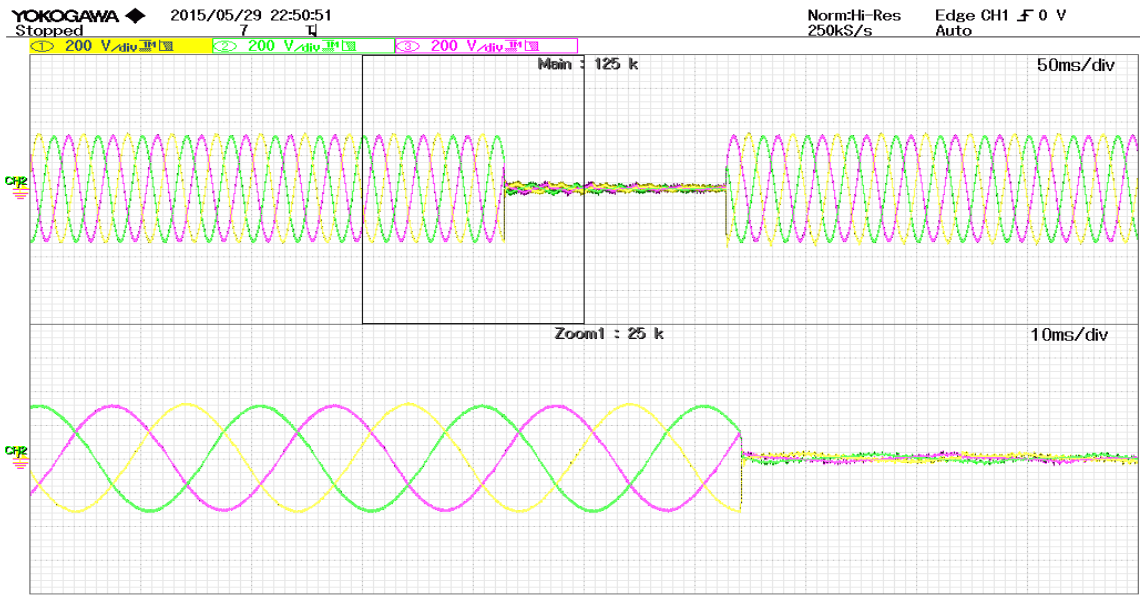


**Figure 27.** Output Voltage sag by 100%.

## 6. Conclusions

In this paper, a good stability and dynamic performance power amplifier has been designed for a PHIL system. The description of various system components of a PHIL system is given. A switch-mode PA, which is based on a compound controller for the rectifier part of a PA, is proposed. It deals with the DC disturbance problem. Moreover, a compound controller, which contains a repetitive controller, is used for the inverter part of a PA. It clearly improves the stability and dynamic performance for a PA.

Experiments under various HUT conditions have been conducted using the designed PA in a PHIL system. The experimental results confirmed the validity of the proposed PHIL system.

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**Author Contributions:** Chenxu Yin and Jianjun Sun designed the main components of the study, including the PHIL model, the compound controller, the analyses of the PHIL system, and the PHIL platform setup. Jinwu Gong and Weiye Chen were responsible for writing the paper. Zhiqiang Liao and Xiaoming Zha mainly worked on the dynamic analyses of the simulated data.

**Conflicts of Interest:** The authors declare no conflict of interest.

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