



Article Four Unity/Variable Gain First-Order Cascaded Voltage-Mode All-Pass Filters and Their Fully Uncoupled Quadrature Sinusoidal Oscillator Applications

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Abstract: This paper presents four new designs for a first-order voltage-mode (VM) all-pass filter (APF) circuit based on two single-output positive differential voltage current conveyors (DVCCs). The first two proposed VMAPFs with unity-gain, high-input (HI) impedance and low-output (LO) impedance use two DVCCs, a grounded capacitor, and a grounded resistor. The last two proposed first-order VMAPFs with HI impedance and variable-gain control are two resistors added to each of the first two VMAPFs. The last two proposed first-order VMAPFs with variable-gain control use two DVCCs, one grounded capacitor, and three grounded resistors and provide HI impedances, so that VMAPFs can be directly cascaded to obtain high-order filters without additional voltage buffers. The four implementation circuits based only on grounded passive components are particularly applicable for integrated circuits (ICs). To confirm the cascading characteristics, an application example of a fully-uncoupled quadrature sinusoidal oscillator (FQSO) is also proposed. PSpice simulation results have confirmed the feasibility of the proposed structures. VMAPF and FQSO circuits are also constructed from commercial AD8130 and AD844 ICs, and their experimentally measured time and frequency responses are compared to theoretical values. The supply voltages for both the AD8130 and AD844 ICs were ± 5 V. The measured power dissipation of the proposed first-order VMAPF and second-order FQSO circuits is 0.6 W. The measured input 1-dB compression point for the four VMAPFs is about 19 dB. The measured total harmonic distortion of the four VMAPFs is less than 0.67% when the input voltage reaches $2.5 V_{pp}$. The calculated figures of merit for the four VMAPFs are 628.2×10^3 , 603.06×10^3 , 516.53×10^3 , and 496.42×10^3 , respectively.

Keywords: first-order filter; oscillator; active circuit; voltage-mode filter; current conveyor

1. Introduction

Voltage-mode (VM) all-pass filters (APFs) are one of the most important components in many sensors, communications, test circuits, and analog signal generation/processing circuits, producing a 180° phase shift and acting as a phase corrector [1–5]. In addition, a quadrature oscillator can be easily implemented by cascading an inverting VMAPF circuit and a non-inverting VMAPF circuit [6]. Many VMAPF circuits have been created in the literature using a single active building block [7–20] or two active building blocks [21–24]. The single active component reported in [7–20] can provide VMAPF circuits, but they require passive component matching conditions to achieve VMAPF circuits. VMAPF circuits based on two active components have also been reported in [21–24], but they do not offer variable-gain control. Four HI impedance VMAPF circuits based on fully differential current conveyor (FDCCII) have been proposed in [25,26], but they still do not offer variablegain control. In addition, the port relationships of the FDCCII are arithmetically equivalent



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Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). to that of two differential difference current conveyor (DDCC) configurations. DDCCbased VMAPF circuits were proposed in [27–32], but they do not provide cascadable fully-uncoupled quadrature sinusoidal oscillator (FQSO) characteristics without adding additional different circuit structures. The circuits proposed in [33–35] have variable-gain control capability, but they require passive component matching conditions to achieve VMAPFs. Some single-output positive and negative differential voltage current conveyor (DVCC+/DVCC-) were reported in [36–40], but they do not offer variable-gain control. To avoid loading issues when cascading VMAPFs into larger systems or to make it easier to connect within a system without additional voltage buffers, VM circuits need HI and LO impedance characteristics. In 2022, two VMAPFs based on single-modified negative DDCC (DDCC–) were proposed in [41]. The first proposed VMAPF in [41] uses a modified DDCC-, two grounded capacitors, and a floating resistor, while the second one uses a grounded capacitor, a grounded resistor, and a floating resistor. Both proposed VMAPFs have HI impedance, but they require passive component matching conditions to achieve the VMAPFs and do not offer variable-gain control and LI impedance. In this paper, four new first-order cascadable VMAPFs with unity/variable-gain control are proposed. The first two VMAPFs employ two DVCCs, one grounded capacitor (GC), and one grounded resistor (GR), while the other two VMAPFs employ two DVCCs, one GC, and three GRs. Positive DVCC configuration is simpler than the dual/negative-type DVCC configuration or the modified DDCC- configuration. Both the first two proposed VMAPFs have HI and LO impedances. Two additional first-order VMAPFs with variable-gain control are also demonstrated by adding two GRs to each of the first two VMAPFs. In addition, the application of cascading two variable-gain control VMAPFs to realize FQSO is also given. An overview of the proposed four VMAPF circuits compared to previously reported circuits is shown in Table 1, which compares their use of active and passive elements, use of only grounded passive elements, unconstrained elements matching, HI impedance, variablegain control, LO impedance, and cascadable synthesis FQSO characteristics without adding additional different circuit structures. In addition to using only grounded passive and unconstrained element matching, the first two circuits have HI and LO impedances, while the latter two circuits have HI impedance and variable-gain control. Furthermore, the last two circuits discussed in this paper for the variable-gain control VMAPFs can be cascaded to synthesize the FQSO without adding another different circuit structure.

Reference	Use of Active and Passive Elements	Use of Only Grounded Passive Elements	Unlimited Passive Matching Conditions	HI/LO Impedance	Variable-Gain Control	Synthesis of FQSO without Adding Different Structures	Simul./Meas.	Supply Voltage	Power Dissipation
[7]	1 CCII–, 2R, 1C	no	no	no/no	no	no	yes/no	NA	NA
[8]	1 CCII+, 2R, 1C	no	no	no/no	no	no	yes/yes	$\pm 12 \text{ V}$	NA
[9]	1 CCII–, 2R, 1C	no	no	no/no	no	no	yes/yes	$\pm 12 \text{ V}$	NA
[10]	1 CCII–, 2R, 1C	no	no	no/no	no	no	yes/yes	$\pm 12 \text{ V}$	NA
[11]	1 DO-CCII, 2R, 1C	no	no	yes/no	no	no	yes/no	$\pm 1.5 \text{ V}$	NA
Figure 3 in [12]	1 DO-CCII, 2 R, 1 C	no	no	yes/no	no	no	yes/no	$\pm 0.75 \text{ V}$	Simul. 1.8 mW
[13]	1 UVC, 2R, 1C	no	no	yes/yes	no	yes	yes/yes	$\pm 2.5 \text{ V}$	Simul. 5.84 mW
[14]	1 UVC, 2R, 1C	yes	no	yes/yes	no	yes	yes/yes	$\pm 1.65 \text{ V}$	NA
[15]	1 ICCII, 2R, 1C	no	no	yes/no	no	no	yes/yes	$\pm 2.5 \text{ V}$	NA
[16]	1 DCCII, 2R, 1C	no	no	no/no	no	no	yes/yes	$\pm 2.5 \text{ V}$	Simul. 14.3 mW
[17]	1 DXCCII, 3R, 1C	yes	no	yes/no	yes	no	yes/no	$\pm 1.25 \text{ V}$	Simul. 2.1 mW
[18]	1 DXCCII, 2R, 1C	no	no	yes/no	no	yes	yes/no	$\pm 1.25 \text{ V}$	Simul. 1.8 mW
[19]	1 CDBA, 3R, 1C	no	no	no/no	no	no	yes/no	$\pm 2.5 \text{ V}$	NA
[20]	1 EX-CCII,2R, 1C	no	no	yes/no	no	no	yes/no	NA	NA
[21]	1 CCII+, 1 CCII–, 4R, 1C	no	no	no/no	no	no	yes/no	NA	NA
[22]	2 CCII+, 2R, 2C	yes	no	yes/no	no	no	no/yes	$\pm 12 \text{ V}$	NA
[23]	2 DVB, 1R, 1C	no	yes	no/yes	no	no	yes/yes	$\pm 0.75 \text{ V}$	Simul. 1.77 mW
[24]	2 OTA, 1R, 1C	yes	no	yes/no	no	no	yes/yes	$\pm 0.4~{ m V}$	Simul. 47.2 µW
[25]	1 FDCCII, 1R, 1C	yes	yes	yes/no	no	yes	yes/no	$\pm 1.3 \text{ V}$	NA
[26]	1 FDCCII, 1R, 1C	yes	yes	yes/yes	no	yes	yes/no	$\pm 3 \text{ V}$	NA
[27]	1 DDCC, 2R, 1C	no	no	yes/no	yes	no	yes/no	$\pm 0.9~{ m V}$	NA
Figure 1 in [28]	1 DDCC, 3R, 1C	no	yes	no/no	yes	no	yes/yes	$\pm 1.25 \text{ V}$	NA
Figure 3 in [28]	2 DDCC, 3R, 1C	yes	yes	yes/no	yes	no	yes/no	$\pm 1.25 \text{ V}$	NA
[29]	1 DDCC, 1R, 1C	no	yes	no/no	no	no	yes/no	$\pm 1.3 \text{ V}$	NA
[30]	1 DDCC, 1R, 1C	no	yes	no/no	no	no	yes/no	$\pm 1.25 \text{ V}$	NA
[31]	1 DDCC, 1R, 1C	no	yes	no/yes	no	no	yes/no	$\pm 3.3 \text{ V}$	NA
Figure 1a in [32]	1 DDCC, 1R, 1C	no	yes	no/no	no	no	yes/no	$\pm 1.5 \text{ V}$	NA
Figure 1b in [32]	2 DDCC, 1R, 1C	yes	yes	yes/no	no	no	yes/no	$\pm 1.5 \text{ V}$	NA
Figure 2 in [33]	2 CFOA, 5R, 1C	no	no	no/yes	yes	no	yes/yes	$\pm 10 \text{ V}$	0.26 W
Figure 3 in [33]	3 CFOA, 5R, 1C	no	no	yes/yes	yes	no	yes/yes	$\pm 10 \text{ V}$	0.39 W

Table 1. An overview of the proposed circuits compared to previously reported VMAPF circuits.

Reference	Use of Active and Passive Elements	Use of Only Grounded Passive Elements	Unlimited Passive Matching Conditions	HI/LO Impedance	Variable-Gain Control	Synthesis of FQSO without Adding Different Structures	Simul./Meas.	Supply Voltage	Power Dissipation
[34]	2 CFOA, 3R, 1C	no	no	yes/yes	yes	no	yes/yes	$\pm 8 \text{ V}$	NA
[35]	1 LT1228	no	no	no/yes	yes	no	yes/yes	$\pm 5 \text{ V}$	57.6 mW
[36]	2 DVCC, 2R, 1C	yes	no	yes/no	no	no	yes/no	$\pm 2.5 \text{ V}$	NA
[37]	2 DVCC, 2R, 1C	yes	no	yes/no	no	no	yes/no	$\pm 2.5 \text{ V}$	NA
[38]	2 DVCC, 1Rx, 1C	yes	yes	no/yes	no	no	yes/no	$\pm 2.5 \text{ V}$	NA
[39]	2 DVCC, 1R, 1C	no	yes	yes/yes	no	no	yes/no	$\pm 1.5 \text{ V}$	Simul. 0.3 W
[40]	2 DVCC, 1R, 1C	yes	yes	yes/no	no	no	yes/no	$\pm 1.25 \text{ V}$	NA
Figure 2 in [41]	1 DDCC, 2C, 1R	no	no	yes/no	no	no	yes/yes	$\pm 1.25 \text{ V}$	Simul. 4.2 mW
Figure 3 in [41]	1 DDCC, 1C, 2R	no	no	yes/no	no	no	yes/yes	$\pm 1.25 \text{ V}$	Simul. 4.21 mW
First proposed 2a in this work	2 DVCC, 1R, 1C	yes	yes	yes/yes	no	yes	yes/yes	$\pm 5 \mathrm{V}$	0.6 W
First proposed 2b in this work	2 DVCC, 1R, 1C	yes	yes	yes/yes	no	yes	yes/yes	$\pm 5 \text{ V}$	0.6 W
Second proposed 3a in this work	2 DVCC, 3R, 1C	yes	yes	yes/no	yes	yes	yes/yes	$\pm 5 \text{ V}$	0.6 W
Second proposed 3b in this work	2 DVCC, 3R, 1C	yes	yes	yes/no	yes	yes	yes/yes	$\pm 5 \mathrm{V}$	0.6 W

Table 1. Cont.

Note: NA: no answer; Simul.: simulation result; Meas.: measurement result; CCII+/CCII-: positive/negative-type second-generation current conveyor; DO-CCII: dual-output second-generation current conveyor; UVC: universal voltage conveyor; ICCII: inverting second-generation current conveyor; DCCII: differential current conveyor; DXCCII: dual-X second-generation current conveyor; CDBA: current differencing buffered amplifier; DVB: subtractor; OTA: operational transconductance amplifier; FDCCII: fully differential second-generation current conveyor; DDCC: differential difference current conveyor; CFOA: current feedback operational amplifier; DVCC: differential voltage current conveyor; HI: high-input; LO: low-output; R: resistor; Rx: X terminal resistance; C: capacitor.

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2. Circuit Description

2.1. Basic Concept of Non-Inverting and Inverting VMAPF Functions

One way to implement the non-inverting and inverting VMAPF functions is to generate the difference functions $V_0(s) = V_{in}(s) - 2V_1(s)$ and $V_0(s) = 2V_1(s) - V_{in}(s)$, respectively, where $V_0(s)$ and $V_{in}(s)$ are the output and input voltages, and $V_1(s)$ is the internal node voltage. If the node voltage $V_1(s)$ realizes the non-inverting first-order low-pass filtering function with the minimum resistor R and capacitor C

$$V_1(s) = \frac{\frac{1}{RC}}{s + \frac{1}{RC}} V_{in}(s)$$
(1)

then the form of the non-inverting and inverting VMAPF functions can be realized as follows:

Non-inverting VMAPF :
$$\frac{V_o(s)}{V_{in}(s)} = \frac{s - \frac{1}{RC}}{s + \frac{1}{RC}}$$
 (2)

Inverting VMAPF:
$$\frac{V_o(s)}{V_{in}(s)} = \frac{-(s - \frac{1}{RC})}{s + \frac{1}{RC}}$$
 (3)

In Equations (1)–(3), the product RC is the time constant of the non-inverting and inverting VMAPF functions. Based on Equations (2) and (3), when the frequency domain $s = j\omega$, and ω is the angular frequency, the gain and phase responses are given by

Non-Inverting VMAPF :
$$\left| \frac{V_{o}(j\omega)}{V_{in}(j\omega)} \right| = 1, \ \angle \varphi_{n} = \pi - 2\arctan(\omega RC)$$
 (4)

Inverting VMAPF:
$$\left| \frac{V_{o}(j\omega)}{V_{in}(j\omega)} \right| = 1, \ \angle \varphi_{i} = -2\arctan(\omega RC)$$
 (5)

Based on Equations (4) and (5), the VMAPF functions maintain a constant gain while shifting the phase of the input signal. The phase characteristic in Equation (4) provides a phase shift between 180° and 0° as the input frequency increases and has a phase shift value of 90° at the pole angular frequency of ω_0 . The phase characteristic in Equation (5) provides a phase shift between 0° and -180° as the input frequency increases and has a phase shift value of -90° at the pole angular frequency of ω_0 . Hence, the non-inverting VMAPF characteristic of the phase shift is a leading phase shifter, and the inverting VMAPF characteristic of the phase shift is a lagging phase shifter. The pole angular frequency ω_0 of the non-inverting and inverting AP filtering functions can be expressed as

$$\omega_{\rm o} = \frac{1}{\rm RC} \tag{6}$$

2.2. Proposed Four VMAPF Circuits and Application Example

The circuit symbol of the DVCC+ and its behavioral model are shown in Figures 1a and 1b, respectively. DVCC+ can be used for a differential voltage and is a variant of current conveyor with a low impedance current input port X, a high impedance current output port Z+, and two high impedance voltage input ports Y_1 and Y_2 .



Figure 1. (a) Circuit symbol and (b) Equivalent circuit of DVCC+.

DVCC+ with differential input impedances is suitable for processing differential signals because it has two HI impedance terminals. The port relationships of the single-output DVCC+ is characterized by the following matrix [42]:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 1 & -1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \end{bmatrix}$$
(7)

According to Equation (7), the voltage $Vx = V_{Y1} - V_{Y2}$ means that the voltage on port X is the differential sensor voltage for the input ports Y_1 and Y_2 . The current $I_Z = I_X$ means that the output current of port Z+ equals the input current of port X. The proposed circuits utilize two DVCCs and two/four grounded passive components. Figures 2a and 2b show the first two proposed VMAPF circuits, respectively, with HI impedance at the input voltage terminal and LO impedance at the output voltage terminal. In Figure 2a,b, the symbol V_{in} is the input voltage; the symbol V_1 is the internal node voltage; the symbols V_{o1} and V_{o2} are the output voltages, and the symbols C_1 , C_2 , R_1 , and R_4 are the capacitors and resistors. Each proposed VMAPF employs two DVCCs, one GC, and one GR, which can be directly cascaded for a higher-order filter without additional voltage buffers. Considering the proposed VMAPF in Figure 2a, the nodal equations can be obtained as:

$$(sC_1R_1 + 1)V_1 = V_{in}$$
(8)

$$V_{o1} = V_{in} - 2V_1 \tag{9}$$



Figure 2. Proposed VMAPFs with HI and LO impedances. (a) Non-inverting APF circuit. (b) Inverting APF circuit.

Solving Equations (8) and (9), the non-inverting APF transfer function can be obtained as:

$$\frac{V_{o1}}{V_{in}} = \frac{s - \frac{1}{C_1 R_1}}{s + \frac{1}{C_1 R_1}} = \frac{s - \omega_o}{s + \omega_o}$$
(10)

Based on Equation (10), the non-inverting APF has a pole angular frequency ω_0 as follows:

U

$$v_{\rm o} = \frac{1}{C_1 R_1} \tag{11}$$

When the capacitor $C_1 = C$ and resistor $R_1 = R$, the gain and phase responses of the non-inverting APF are the same as given in Equation (4).

Considering the proposed VMAPF in Figure 2b, the nodal equations can be obtained as:

$$(sC_2R_4 + 1)V_1 = V_{in}$$
(12)

$$V_{o2} = 2V_1 - V_{in}$$
(13)

Solving Equations (12) and (13), the inverting APF transfer function can be obtained as:

$$\frac{V_{o2}}{V_{in}} = \frac{-(s - \frac{1}{C_2 R_4})}{s + \frac{1}{C_2 R_4}}$$
(14)

According to Equation (14), the pole angular frequency of the inverting APF is $\omega_0 = 1/C_2R_4$. When the capacitor $C_2 = C$ and resistor $R_4 = R$, the gain and phase responses of the inverting APF are the same as given in Equation (5).

According to Equations (10) and (14), both the non-inverting APF and the inverting APF have unity-gain. By adding two GRs to the first two VMAPFs in Figures 2a and 2b, respectively, two other first-order VMAPFs with HI impedance and variable-gain control were realized, as shown in Figures 3a and 3b, respectively. In Figure 3a,b, the symbol V_{in} is the input voltage; the symbols V₀₃ and V₀₄ are the output voltages, and the symbols C₁, C₂, R₁, R₂, R₃, R₄, R₅, and R₆ are capacitors and resistors.



Figure 3. Proposed VMAPF with HI impedance and variable-gain control. (**a**) Non-inverting APF circuit. (**b**) Inverting APF circuit.

The analysis of Figure 3a leads to the non-inverting APF transfer function as follows:

$$\frac{V_{o3}}{V_{in}} = \left(\frac{R_3}{R_2}\right) \left(\frac{s - \frac{1}{C_1 R_1}}{s + \frac{1}{C_1 R_1}}\right) = k_1 \left(\frac{s - \omega_1}{s + \omega_1}\right)$$
(15)

Based on Equation (15), the non-inverting APF has the following pole angular frequency ω_1 and variable-gain control k₁:

$$\omega_1 = \frac{1}{C_1 R_1}, \ k_1 = \frac{R_3}{R_2} \tag{16}$$

Similarly, the analysis of Figure 3b leads to the inverting APF transfer function as follows:

$$\frac{V_{o4}}{V_{in}} = -(\frac{R_6}{R_5})(\frac{s - \frac{1}{C_2 R_4}}{s + \frac{1}{C_2 R_4}}) = -k_2(\frac{s - \omega_2}{s + \omega_2})$$
(17)

Based on Equation (17), the inverting APF has the following pole angular frequency ω_2 and variable-gain control k_2 :

$$\omega_2 = \frac{1}{C_2 R_4}, \ k_2 = \frac{R_6}{R_5} \tag{18}$$

Thus, each structure proposed in Figure 3a,b has variable-gain control without affecting the pole angular frequency. Since the circuits of Figure 3a,b have HI impedance, the VM FQSO can be easily implemented by cascading the proposed non-inverting VMAPF and inverting VMAPF circuits without adding additional different circuit structures. To confirm the cascading characterizing of Figure 3a,b, the VM FQSO is implemented using variable-gain control of the proposed non-inverting and inverting APFs. Figure 4 shows the application of the proposed VMAPFs to synthesize a VM FQSO by cascading a noninverting APF transfer function and an inverting APF transfer function with variable-gain control into the feedback loop.



Figure 4. Block diagram of a FQSO by cascading a variable-gain control non-inverting APF transfer function and an inverting APF transfer function.

Based on the cascaded non-inverting and inverting APF transfer functions of Figure 4, the characteristic equation (CE) can be obtained.

CE:
$$s^2 + s(\omega_1 + \omega_2)(\frac{1 - k_1 k_2}{1 + k_1 k_2}) + \omega_1 \omega_2 = 0$$
 (19)

where $\omega_1 = \frac{1}{R_1C_1}$, $\omega_2 = \frac{1}{R_4C_2}$, $k_1 = \frac{R_3}{R_2}$, and $k_2 = \frac{R_6}{R_5}$.

According to Equation (19), the frequency of oscillation (FO) and the condition of oscillation (CO) are

FO:
$$f_o = \frac{1}{2\pi} \sqrt{\frac{1}{R_1 R_4 C_1 C_2}}$$
 (20)

$$CO: \ 1 \le (\frac{R_3}{R_2})(\frac{R_6}{R_5})$$
(21)

Examining Equations (20) and (21), FO and CO are fully decoupled. Therefore, FO can be independently adjusted by R_1 and R_4 , and CO can be independently adjusted by R_2 , R_3 , R_5 , and R_6 . Using the oscillator building blocks in Figure 4, Figure 5 shows how the non-inverting and inverting APFs of Figure 3a,b can be cascaded to synthesize the VM FQSO, CE, FO, and CO derived from Figure 5 are the same as Equations (19), (20), and (21), respectively.



Figure 5. The quadrature sinusoidal oscillator based on cascading a non-inverting APF and an inverting APF with variable-gain control.

3. Simulation Results

To validate the theoretical analyses, simulations were performed using PSpice, and experimental measurements were performed using AD8130 [43,44] and AD844 [45] commercially available components to determine the feasibility and accuracy of the proposed first-order VMAPFs and second-order FQSO. The supply voltages for both the AD8130 and AD844 were ± 5 V. Figure 6 shows a possible equivalent implementation using Analog Devices AD8130 and AD844 ICs instead of DVCC+. To obtain f₀ = 62.41 kHz, a grounded capacitor of 510 pF and a grounded resistance of 5 k Ω were chosen in Figure 2a,b. Figures 7 and 8 show the simulated gain and phase frequency responses of the first two proposed circuits for the unity-gain of the non-inverting VMAPF and the inverting VMAPF in Figures 2a and 2b, respectively. For the non-inverting VMAPF pole frequency with a theoretical phase shift of 90°, the simulated pole frequency with a theoretical phase shift of 90°, the simulated pole frequency with a theoretical phase shift of 90°, the simulated pole frequency with a theoretical phase shift of 90° the simulated pole frequency with a theoretical phase shift of 90°, the simulated pole frequency with a theoretical phase shift of 90° the simulated pole frequency with a theoretical phase shift of 90° the simulated pole frequency with a theoretical phase shift of 90° the simulated pole frequency with a theoretical phase shift of 90° the simulated pole frequency with a theoretical phase shift of 90° the simulated pole frequency with a theoretical phase shift of 90° the simulated pole frequency with a theoretical phase shift of 90° the simulated pole frequency with a theoretical phase shift of 90° the simulated pole frequency with a theoretical phase shift of -1.6 kHz. For the inverting VMAPF pole frequency with a theoretical phase shift of -90° the simulated pole frequency in Figure 8 is 60.95 kHz with an offset of -1.46 kHz.



Figure 6. A possible implementation of the DVCC+ using AD8130 and AD844 ICs.

20

10

0

Gain, dB





Figure 7. Simulated gain and phase frequency response of the non-inverting VMAPF of Figure 2a.



Figure 8. Simulated gain and phase frequency response of the inverting VMAPF of Figure 2b.

A single grounded capacitor of 510 pF and three equal grounded resistors of 5 k Ω , and the last two proposed variable-gain control non-inverting and inverting VMAPF circuits, shown in Figure 3a,b, were designed for $f_0 = 62.41$ kHz. To verify the last two proposed variable-gain control non-inverting and inverting VMAPF circuits in Figure 3a,b, Figures 9 and 10 show the frequency domain simulations of the non-inverting and inverting VMAPFs with an ideal pole frequency of 62.41 kHz, respectively. For a non-inverting VMAPF pole frequency with a theoretical phase shift of 90°, the simulated pole frequency with a theoretical phase shift of 90°, the simulated pole frequency with a theoretical phase shift of -2.11 kHz. For an inverting VMAPF pole frequency with a theoretical phase shift of -90° , the simulated pole frequency in Figure 10 is 60.5 kHz, and the offset is -1.91 kHz.



Figure 9. Simulated gain and phase frequency response of the variable-gain control non-inverting VMAPF of Figure 3a.



Figure 10. Simulated gain and phase frequency response of the variable-gain control inverting VMAPF of Figure 3b.

4. Experimental Results

To measure the gain and phase responses of the first-order VMAPF in the frequency domain, the receiver resolution bandwidth of the Keysight E5061B-3L5 network analyzer was fixed at 100 Hz. To measure circuits in time-domain input/output waveforms, the Tektronix AFG1022 signal generator applied 2.5 V_{PP} to the first-order VMAPF circuits and used an oscilloscope Tektronix DPO 2048B to measure. The Keysight-Agilent N9000A signal analyzer evaluated third-order intermodulation distortion (IMD3), third-order intercept (TOI), phase noise (PN), total harmonic distortion (THD), spurious-free dynamic range (SFDR), and 1-dB compression point (P1dB) analysis. Figure 11 shows photographs of the top and bottom views of the non-inverting and inverting first-order VMAPFs or FQSO printed circuit board (PCB) hardware implementation. Figure 12 shows the photograph of the hardware setup used to experimentally verify the performance of the proposed circuits and shows the gain and phase responses in the frequency of the non-inverting VMAPF as a test case. The supply voltages for both the AD8130 and AD844 are \pm 5 V. The measured power dissipation of the proposed first-order VMAPF and second-order FQSO circuits is 0.6 W.



Figure 11. Photographs of the PCB hardware (**a**) top view and (**b**) bottom view for the non-inverting and inverting first-order VMAPFs or second-order FQSO.



Figure 12. The photograph of the hardware setup used to verify the performance of the proposed non-inverting VMAPF.

To obtain $f_0 = 62.41$ kHz, a grounded capacitor of 510 pF and a grounded resistance of 5 k Ω were chosen in Figure 2a,b. Figures 13 and 14 show the measured gain and phase frequency responses of the first two proposed circuits for the unity-gain of the noninverting VMAPF and the inverting VMAPF in Figures 2a and 2b, respectively. For the non-inverting VMAPF pole frequency with a theoretical phase shift of 90°, the measured pole frequency in Figure 13 is 65.29 kHz with an offset of 2.88 kHz. For the inverting VMAPF pole frequency with a theoretical phase shift of -90° , the measured pole frequency in Figure 14 is 65.09 kHz with an offset of 2.68 kHz. Figures 15 and 16 show the measured time-domain input/output waveforms of the non-inverting and inverting VMAPF circuits of Figures 2a and 2b, respectively. At the pole frequency shown in Figure 15, the theoretical phase shift of the first-order non-inverting VMAPF is 90°; the measured phase shift is 89.81°, and the phase error is -0.19° . At the pole frequency shown in Figure 16, the theoretical phase shift of the first-order inverting VMAPF is -90° ; the measured phase shift is -88.15° , and the phase error is 1.85° .



Figure 13. The frequency domain of the non-inverting VMAPF in Figure 2a with the starting frequency range from 1 kHz to 1 MHz.



Figure 14. The frequency domain of the inverting VMAPF in Figure 2b with the starting frequency range from 1 kHz to 1 MHz.



Figure 15. The time domain of the non-inverting VMAPF in Figure 2a with an input signal of $2.5 V_{pp}$ at 62.41 kHz. (a) Input/output signals. (b) X–Y plot.





Figure 16. The time domain of the inverting VMAPF in Figure 2b with an input signal of 2.5 V_{pp} at 62.41 kHz. (a) Input/output signals. (b) X–Y plot.

A single grounded capacitor of 510 pF and three equal grounded resistors of 5 k Ω and the last two proposed variable-gain control non-inverting and inverting VMAPF circuits shown in Figure 3a,b, are designed for $f_0 = 62.41$ kHz. To verify the last two proposed variable-gain control non-inverting and inverting VMAPF circuits in Figure 3a,b, Figures 17 and 18 show the frequency domain measurements of the non-inverting and inverting VMAPFs with an ideal pole frequency of 62.41 kHz, respectively. For a noninverting VMAPF pole frequency with a theoretical phase shift of 90°, the measured pole frequency in Figure 17 is 62.22 kHz with an offset of -0.19 kHz. For an inverting VMAPF pole frequency with a theoretical phase shift of -90° , the measured pole frequency in Figure 18 is 63.78 kHz, and the offset is 1.37 kHz. Figures 19 and 20 show input/output waveforms in the time domain for the non-inverting and inverting VMAPF circuits of Figures 3a and 3b, respectively. At the pole frequency shown in Figure 19, the theoretical phase shift of the first-order non-inverting VMAPF is 90°; the measured phase shift is 88.48°, and its phase error is -1.52° . At the pole frequency shown in Figure 20, the theoretical phase shift of the first-order inverting VMAPF is -90° ; the measured phase shift is -93.26° , and its phase error is -3.26° .



Figure 17. The frequency domain of the non-inverting VMAPF in Figure 3a with the starting frequency range from 1 kHz to 1 MHz.



Figure 18. The frequency domain of the inverting VMAPF in Figure 3b with the starting frequency range from 1 kHz to 1 MHz.



Figure 19. The time domain of the non-inverting VMAPF in Figure 3a with an input signal of 2.5 V_{pp} at 62.41 kHz. (**a**) Input/output signals. (**b**) X–Y plot.



Figure 20. The time domain of the inverting VMAPF in Figure 3b with an input signal of 2.5 V_{pp} at 62.41 kHz. (a) Input/output signals. (b) X–Y plot.

To evaluate the THD, SFDR, IMD3, TOI, PN, and P1dB analysis of the proposed VMAPFs, the proposed paper investigated linearity, dynamic range, harmonic content, mixed, intermodulation linearity, phase noise analysis, and input power range. Figures 21 and 22 show the frequency spectrum of Figures 2a and 2b, respectively. In Figure 21, the calculated THD and measured SFDR values are 0.23% and 57.73 dB, respectively. In Figure 22, the calculated THD and measured SFDR values are 0.29% and 55.59 dB, respectively. Figures 23 and 24 show the THD analysis measured by the operating frequency of 62.41 kHz and the varying input voltage in Figures 2a and 2b, respectively. As shown in Figures 23 and 24, the measured THD is less than 1.13% when the input voltage signal reaches 3.5 V_{pp} .

Figures 25 and 26 show the frequency spectrum of Figures 3a and 3b, respectively. In Figure 25, the calculated THD and measured SFDR values are 0.5% and 49.81 dB, respectively. In Figure 26, the calculated THD and measured SFDR values are 0.67% and 46.7 dB, respectively. Figures 27 and 28 show the measured THD analysis at an operating frequency of 62.41 kHz versus the varying input voltage in Figures 3a and 3b, respectively. As shown in Figures 27 and 28, the measured THD is less than 1.6% when the input voltage signal reaches $3.5 V_{pp}$. Figures 29–32 show the intermodulation linearity of the two-tone tests with $f_1 = 61.41$ kHz for the low-frequency tone and $f_2 = 63.41$ kHz for the high-frequency tone, respectively. In Figure 29, the measured IMD3 and TOI of Figure 2a are -57.42 dBc and 33.18 dBm, respectively. In Figure 30, the measured IMD3 and TOI of Figure 2b are -63.91 dBc and 35.18 dBm, respectively. In Figure 31, the measured IMD3 and TOI of Figure 3a are -65.69 dBc and 36.45 dBm, respectively. In Figure 32, the measured IMD3 and TOI of Figure 3b are -52.12 dBc and 31.1 dBm, respectively. Figures 33-36 show the PN analysis of approximately 11.6 dBm input carrier power. In Figure 33, the PN measured of Figure 2a at an offset of 100 Hz is -88.61 dBc/Hz. In Figure 34, the PN measured of Figure 2b at an offset of 100 Hz is -89.07 dBc/Hz. In Figure 35, the PN measured of Figure 3a at an offset of 100 Hz is -84.38 dBc/Hz. In Figure 36, the PN measured of Figure 3b at an offset of 100 Hz is -82.68 dBc/Hz. Figures 37-40 show the input power range for P1dB, respectively. In Figure 37, the input P1dB of Figure 2a is 19.6 dBm. In Figure 38, the input P1dB of Figure 2b is 19.4 dBm. In Figure 39, the input P1dB of Figure 3a is 19 dBm. In Figure 40, the input P1dB of Figure 3b is 19.6 dBm.



Figure 21. Fourier spectrum of Figure 2a with an input signal of 2.5 V_{pp} at 62.41 kHz.



Figure 22. Fourier spectrum of Figure 2b with an input signal of 2.5 V_{pp} at 62.41 kHz.



Figure 23. THD measured analysis versus the varying input voltages applied in Figure 2a.



Figure 24. THD measured analysis versus the varying input voltages applied in Figure 2b.



Figure 25. Fourier spectrum of Figure 3a with an input signal of 2.5 V_{pp} at 62.41 kHz.



Figure 26. Fourier spectrum of Figure 3b with an input signal of 2.5 V_{pp} at 62.41 kHz.



Figure 27. THD measured analysis versus the varying input voltages applied in Figure 3a.



Figure 28. THD measured analysis versus the varying input voltages applied in Figure 3b.



Figure 29. Output spectrum of the two-tone intermodulation distortion test of Figure 2a.



Figure 30. Output spectrum of the two-tone intermodulation distortion test of Figure 2b.



Figure 31. Output spectrum of the two-tone intermodulation distortion test of Figure 3a.



Figure 32. Output spectrum of the two-tone intermodulation distortion test of Figure 3b.



Figure 33. PN analysis of Figure 2a at approximately 11.64 dBm input carrier power.



Figure 34. PN analysis of Figure 2b at approximately 11.68 dBm input carrier power.



Figure 35. PN analysis of Figure 3a at approximately 11.3 dBm input carrier power.



Figure 36. PN analysis of Figure 3b at approximately 11.3 dBm input carrier power.



Figure 37. P1dB analysis of Figure 2a.



Figure 38. P1dB analysis of Figure 2b.



Figure 39. P1dB analysis of Figure 3a.



Figure 40. P1dB analysis of Figure 3b.

To evaluate the performance of the proposed VMAPF, the figure of merit (FoM) is defined as [42]

$$FoM = \frac{Dynamic Range \times f_o}{Power Disspation \times Supply Voltage}$$
(22)

According to Equation (22), the FoM of the VMAPFs presented in Figure 2a, Figure 2b, Figure 3a, and Figure 3b are 628.2×10^3 , 603.06×10^3 , 516.53×10^3 , and 496.42×10^3 , respectively. The summary performance of the proposed VMAPFs is given in Table 2.

Table 2. Performance parameters of the proposed VMAPFs.

Parameter	Figure 2a in This Work	Figure 2b in This Work	Figure 3a in This Work	Figure 3b in This Work	
Power supply	\pm 5 V	$\pm 5 \text{ V}$	$\pm 5 \text{ V}$	$\pm 5 \text{ V}$	
Power dissipation	0.6 W	0.6 W	0.6 W	0.6 W	
Pole frequency (@ frequency domain)	65.29 kHz	65.09 kHz	62.22 kHz	63.78 kHz	
Phase error (@ time domain)	-0.19°	1.85°	-1.52°	-3.26°	
THD (@Vin = $2.5 V_{pp}$)	0.23%	0.28%	0.5%	0.67%	
SFDR	57.73 dB	55.59 dB	49.81 dB	46.7 dB	
Input P1dB	19.6 dB	19.4 dB	19 dB	19.6 dB	
TOI	33.18 dBm	35.18 dBm	36.45 dBm	31.1 dBm	
IMD3	-57.42 dBc	-63.91 dBc	-65.69 dBc	-52.12 dBc	
PN (@100 Hz offset)	-88.61 dBc/Hz	−89.07 dBc/Hz	-84.38 dBc/Hz	-82.68 dBc/Hz	
FoM	628.2×10^3	603.06×10^{3}	516.53×10^{3}	496.42×10^{3}	

To confirm the cascading characteristics, an application example of FQSO in Figure 5 was also studied. The FQSO in Figure 5 was designed with equal capacitor of value 510 pF, $R_1 = R_2 = R_4 = R_5 = R_6 = 5 \text{ k}\Omega$, and $R_3 = 6.2 \text{ k}\Omega$. Figure 41 shows the time domain measurements of the quadrature sinusoidal outputs V_{o1} and V_{o2} , and the measured oscillation frequency is 59.05 kHz, which is close to the theoretical value of 62.41 kHz. The Fourier spectrum of the quadrature outputs is shown in Figures 42a and 42b, respectively. In Figure 42a, the calculated THD and measured SFDR of V_{o1} output value are 0.8% and 42.88 dB, respectively. In Figure 42b, the calculated THD and measured of FQSO is shown in Figures 43a and 43b, respectively. At an offset of 100 Hz, the measured V_{o1} and V_{o2} PN are -32.32 dBc/Hz and -32.98 dBc/Hz, respectively. Figure 44 shows the experimental results of the oscillation frequencies of Figure 5 by varying the values of $R_1 = R_4$ with the equal capacitor of value 510 pF, $R_2 = R_5 = R_6 = 5 \text{ k}\Omega$, and $R_3 = R_6 = 6.2 \text{ k}\Omega$.



Figure 41. Time domain of FQSO. (a) quadrature sinusoidal outputs V_{o1} and V_{o2} . (b) X–Y plot.



Figure 42. Fourier spectrum of quadrature sinusoidal output signals. (a) V_{o1} output spectrum. (b) V_{o2} output spectrum.



Figure 43. The measured PN of the proposed FQSO. (a) V_{o1} output terminal. (b) V_{o2} output terminal.



Figure 44. The experimental results of the oscillation frequencies of Figure 5 by varying the values of $R_1 = R_4$ with $C_1 = C_2 = 510$ pF, $R_2 = R_5 = R_6 = 5$ k Ω , and $R_3 = 6.2$ k Ω .

5. Comparison of VMAPF Theoretical, Simulation, and Experimental Results

To demonstrate the theoretical study of the four VMAPFs, the theoretical analysis of Equations (10), (14), (15) and (17) was performed using Matlab version R2014a software. To evaluate the feasibility of the four VMAPFs, Figure 2a,b and Figure 3a,b were simulated using Cadence OrCAD PSpice version 17.2. To confirm the utility of the four VMAPFs, measurements of the four VMAPFs were performed in Figure 11. Figures 45 and 46 show the theoretical analysis in Matlab and the simulated and measured responses of the first two proposed non-inverting and inverting VMAPF circuits, respectively. Figures 47 and 48 show the simulation and measurement responses of the last two proposed variable-gain control non-inverting and inverting VMAPF circuits, as well as the theoretical analysis in Matlab. In order to illustrate the adjustable features of circuits in Figure $3a_{1}b_{2}$, R_{3} and R_{6} were changed to $3.15 \text{ k}\Omega$, $6.3 \text{ k}\Omega$, $10 \text{ k}\Omega$, and $15.8 \text{ k}\Omega$ to obtain -4 dB, 2 dB, 6 dB, and 10 dBcorresponding gains, while maintaining $C_1 = C_2 = 510$ pF and $R_1 = R_2 = R_4 = R_5 = 5k\Omega$. Figures 49 and 50 show the theoretical analysis in Matlab and the simulated and measured variable-gain control without affecting the phase responses in Figures 3a and 3b, respectively. In order to illustrate the adjustable characteristics of the structure displayed, R_1 in Figure 3a and R₄ in Figure 3b were changed to 2.5 k Ω , 4 k Ω , 7.5 k Ω , and 15 k Ω to obtain 124.82 kHz, 78.43 kHz, 41.6 kHz, and 20.8 kHz corresponding to fo, while maintaining $C_1 = C_2 = 510 \text{ pF}$ and $R_2 = R_3 = R_5 = R_6 = 5 \text{ k}\Omega$. Figures 51 and 52 show the theoretical analysis in Matlab and the simulated and measured tunable phase response without affecting the gain in Figures 3a and 3b, respectively. These results show that each structure proposed in Figure 3a,b has variable-gain control without affecting the pole frequency. The experimental and simulation results show that Figures 45 and 52 are in good agreement with the predicted theory, confirming the feasibility of the four proposed VMAPF configurations. However, the differences among the theoretical, simulated, and measured results of the four proposed VMAPFs mainly come from the parasitic impedance effects of active components, passive component tolerances, and PCB circuit layout. To evaluate the difference in the phase shift results of the active and passive components, the sensitivity of the pole angular frequency ω_0 and gain k parameters of the VMAPF with respect to the passive components of R and C were analyzed using the sensitivity definitions. The sensitivity is defined as [28]

$$S_{\rm X}^{\rm F} = \frac{{\rm x}}{{\rm F}} \frac{\partial {\rm F}}{\partial {\rm x}} \tag{23}$$



Figure 45. The theoretical analysis in Matlab and the simulated and measured responses of Figure 2a.



Figure 46. The theoretical analysis in Matlab and the simulated and measured responses of Figure 2b.



Figure 47. The theoretical analysis in Matlab and the simulated and measured responses of Figure 3a.







Figure 49. Gain tunability of Figure 3a.



Figure 50. Gain tunability of Figure 3b.



Figure 51. Tunability of pole frequency of Figure 3a.



Figure 52. Tunability of pole frequency of Figure 3b.

In Equation (23), F represents one of the pole angular frequencies ω_0 ; the gain is k, and x represents the passive component of resistor R or capacitor C. Based on Equation (23), the low passive sensitivity of the four VMAPFs is calculated as

Non-inverting unity-gain VMAPF :
$$S_{R_1}^{\omega_o} = S_{C_1}^{\omega_o} = -1$$
 (24)

Inverting unity-gain VMAPF :
$$S_{R_4}^{\omega_0} = S_{C_2}^{\omega_0} = -1$$
 (25)

Non-inverting variable-gain VMAPF :
$$S_{R_1}^{\omega_o} = S_{C_1}^{\omega_o} = -1$$
, $S_{R_2}^k = -1$, $S_{R_3}^k = 1$ (26)

Inverting variable-gain VMAP :
$$S_{R_4}^{\omega_0} = S_{C_2}^{\omega_0} = -1$$
, $S_{R_5}^k = -1$, $S_{R_6}^k = 1$ (27)

According to Equations (24)-(27), the four proposed VMAPFs have a low passive sensitivity.

6. Conclusions

In 2022, Abaci et al. proposed two VMAPFs based on single-modified DDCC–. The first proposed VMAPF uses a modified DDCC–, two grounded capacitors, and a floating resistor, while the second one uses a grounded capacitor, a grounded resistor, and a floating resistor. Both proposed VMAPFs have HI impedance, but they require passive component matching conditions to achieve the VMAPFs and do not offer variable-gain control and LI impedance. In this paper, four new designs for a first-order VMAPF circuit based

on two DVCCs are presented. The four proposed VMAPF circuits offer the following attractive features simultaneously: (i) Only GC and GR are used to absorb shunt parasitic capacitances and resistances. (ii) The HI impedance is easily cascaded with other VM circuits without the need for an input voltage buffer. (iii) Inverting APF and non-inverting APF functions do not require matching conditions for passive components. In addition, the first two proposed VMAPFs with LO impedance are beneficial for output cascading, and the latter two proposed VMAPFs with variable-gain control are beneficial for filter-gain controllability. Furthermore, the application as FQSO by cascading the inverting APF and non-inverting APF techniques is discussed. The measured input 1-dB compression point of the four VMAPFs is about 19 dB. The measured THD of the four VMAPFs is less than 0.67% when the input voltage reaches 2.5 V_{pp}. The calculated figures of merit for the four VMAPFs are 628.2×10^3 , 603.06×10^3 , 516.53×10^3 , and 496.42×10^3 , respectively. The simulation and measurement results are consistent with theoretical predictions.

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