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Reducing Measurement Time in Direct Interface Circuits for Resistive Sensor Readout

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Abstract: Direct Interface Circuits (DICs) carry out resistive sensor readings using a resistance-to-time-to-digital conversion without the need for analog-to-digital converters. The main advantage of this approach is the simplicity involved in designing a DIC, which only requires some additional resistors and a capacitor in order to perform the conversion. The main drawback is the time needed for this conversion, which is given by the sum of up to three capacitor charge times and their associated discharge times. This article presents a modification of the most widely used estimation method in a resistive DIC, which is known as the Two-Point Calibration Method (TPCM), in which a single additional programmable digital device pin in the DIC and one extra measurement in each discharge cycle, made without slowing down the cycle, allow charge times to be reduced more than 20-fold to values around 2 μ s. The new method designed to achieve this reduction only penalizes relative errors with a small increase of between 0.2% and 0.3% for most values in the tested resistance range.

Keywords: direct interface circuits; calibration methods; error analysis; resistive sensor; interface sensor; time-based measurement

1. Introduction

Electrical magnitudes of sensors can currently be read using a wide range of circuits, including Direct Interface Circuits (DICs), which comprise several features that make them particularly suitable for multiple applications. A DIC performs a magnitude-to-time-to-digital conversion through a programmable digital device (PDD) and a few additional elements. The first versions of DICs were proposed, almost simultaneously, by Sherman and Webjörn [1,2].

Reading a sensor with a DIC produces a digital output that can be processed directly by the same PDD as used for the measurement, without the need for analog-to-digital conversion. Indeed, only a few simple extra elements are required, such as resistors, capacitors, transistors, or triggers [3]. Such simplicity means that this type of circuit is particularly suited for portable applications, where both the number of components and their consumption are very important. DICs are also highly versatile in terms of the PDDs used, allowing the use of both microcontrollers [4–10] and field-programmable gate arrays (FPGAs) [11–16]. The calculation capabilities of a PDD connected to a DIC allow them to function as smart sensors, pre-processing information from the sensor and thus reducing the workload in subsequent high-level processing and decision stages [17].

Although there are DICs for reading both capacitive and inductive sensors, those for resistive sensors have probably been the most widely used and analyzed in the literature, whether individually [3,7,18,19] or grouped in arrays [11,14]. Several issues need to be considered when designing a resistive DIC, such as accuracy, uncertainty, resolution [6,8,16,20–22], and calibration

points [23]. Other problems that may influence the performance of these circuits such as response to dynamic signals [24], lead wire resistance [25], power consumption [5], estimation time [13], or problems related to the measurement of low-resistance sensors [15], have also been addressed.

However, problems related to variations in the charge voltage on the capacitor used in a resistive DIC have not received as much attention in the literature. These variations are fundamentally related to two causes. Firstly, there is the interference effect of the power supply in the voltage stored on the capacitor. This effect has only been studied in [26]. This article showed how results can be improved when charging the capacitor through an additional resistor connected to a PDD output and to the capacitor itself. Nevertheless, this solution presents a new problem, namely the increase in charge time due to the presence of this resistor. Secondly, the length of this charge time limits the operation of a resistive DIC in relation to the capacitor's final charge voltage, since precise measurements can only be achieved if the capacitor's different charges (as necessary in the resistive sensor reading process) reach the same voltage; this means a high charge time is required, thus minimizing any differences in the initial charge voltages [27] showed that the charge time must be at least five times the time constant formed, firstly, by the sum of the additional resistance and the resistance presented by a PDD output buffer, and, secondly, by the capacitor. Thus, if $T_E(R_S)$ refers to the total time for estimating the resistance value of a sensor, R_S , this time will increase notably due to this additional resistance, which, even when it has a small value as in [26], will always be much higher than the PDD buffer's small output resistance value.

This article will set out a new method to offset the effects of variations in the final voltage on the capacitor charge cycles of a resistive DIC. This new method can be used to reduce errors when estimating the resistance value of the sensor due to this reason, or to reduce the capacitor's charge time, thus decreasing $T_E(R_S)$.

The structure of the paper is as follows. Section 2 shows the operating principles of the different types of DICs and their fundamental characteristics. Section 3 presents the new DIC proposal. Section 4 shows the materials and methods used in the evaluation of the new proposal and the experimental results. Finally, the conclusions are presented in Section 5.

2. Operating Principle of a DIC

The DIC most frequently used in the literature for reading resistive sensors uses the Two-Point Calibration Method, TPCM. This has the structure shown in Figure 1a. The R_S reading process consists of three cycles. In the first part of each cycle, capacitor C is charged to a voltage, V_{ch} , which is ideally equal to the supply voltage, V_{DD} . This is done by placing a logic 1 output in the PDD's Pp pin and charging C through resistor R_p (added in accordance with the indications of [26]). During the charge process, pins Ps, Pc1, and Pc2 are in a high-impedance state, HZ (i.e., configured as inputs). Then, the discharge of C takes place by placing the logic 0 output in one of the PDD's Ps, Pc1, and Pc2 pins. Only one of these three pins will be configured as logic 0 output during the discharge processes, with the other two and Pp configured in the HZ state. Therefore, one discharge takes place through R_S , and the other two take place through two known calibration resistors, R_{C1} and R_{C2} . The voltage of the capacitor, $V_C(t)$, will evolve according to the following equation during the discharge process through R_S :

$$V_C(t) = V_{ch} e^{\frac{-t}{(R_S + R_o)C}} \quad (1)$$

where R_o is the output resistance of each pin configured as logic 0 output. The discharge ends when it is detected that the voltage in C has dropped below the threshold voltage V_{Th} of the Pp pin (configured as input). Equation (1) can be used to establish the time taken in this discharge, T_{R_S} :

$$T_{R_S} = (R_S + R_o)C \ln\left(\frac{V_{ch}}{V_{Th}}\right) \quad (2)$$

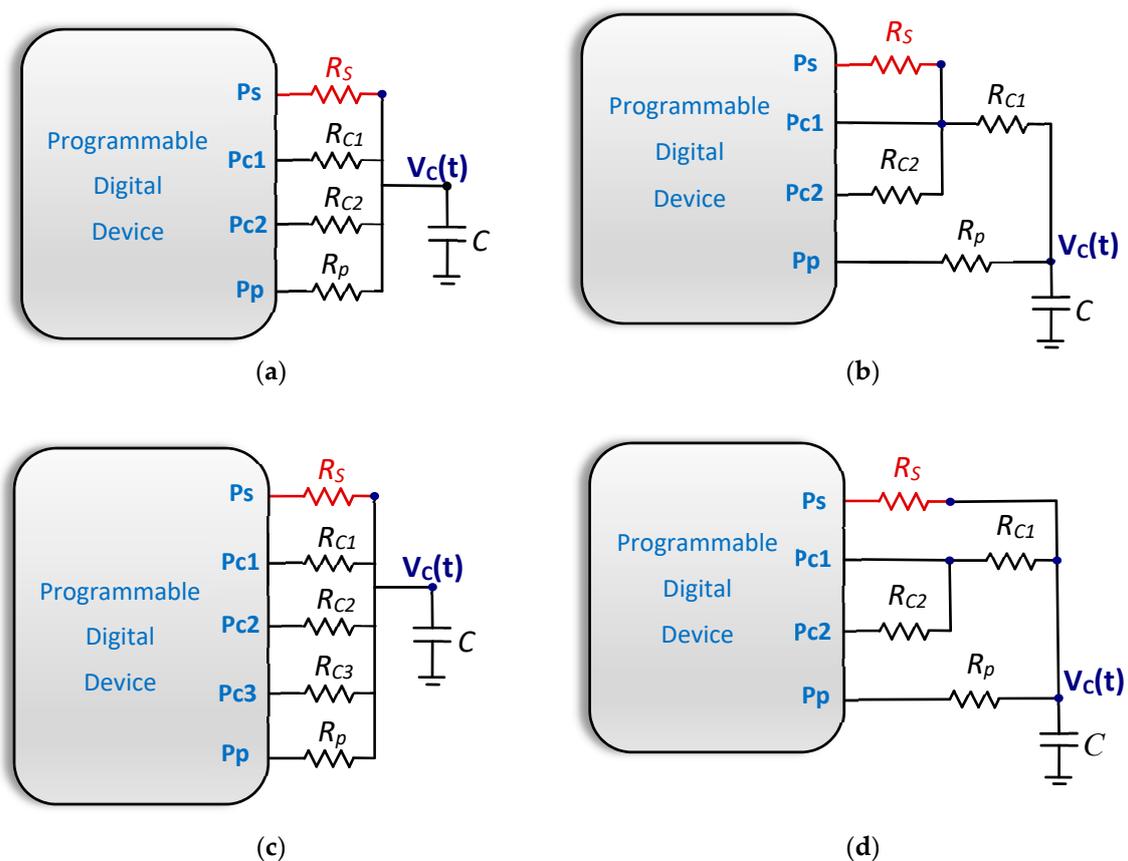


Figure 1. Different types of resistive Direct Interface Circuits (DICs) proposed in the literature (resistor/sensor to be estimated shown in red). (a) Two-Point Calibration Method, TPCM. (b) Three-Signal Method, TSM. (c) DIC for measuring low resistance values. (d) DIC designed to reduce quantization error.

Discharging through R_{C1} and R_{C2} instead of through R_S achieves times T_{Rc1} and T_{Rc2} , replacing R_S with R_{C1} and R_{C2} in Equation (2). If the noise in V_{DD} is low and the charge times are long enough for discharges to always start from the same voltage on the capacitor, $V_{ch} \approx V_{DD}$, then the value of R_S can be expressed straightforwardly in accordance with these times [4]:

$$R_S = \frac{T_{R_S} - T_{Rc1}}{T_{Rc2} - T_{Rc1}} (R_{C2} - R_{C1}) + R_{C1} \quad (3)$$

This is the known equation for finding R_S in the TPCM. The times shown in this equation represent integers of the PDD clock period, T_{CK} . Therefore, R_S can be found through known resistance values and the three-time measurement, eliminating dependence on C , V_{ch} , and V_{Th} .

A variant of this resistive DIC, which uses the same passive components (although arranged differently) and a different calibration method, is the Three Signals Method or TSM, as shown in Figure 1b. Three charge–discharge cycles are also carried out in the TSM, although in this case, discharge (duly configuring the pins) takes place through R_{C1} , $R_{C2} + R_{C1}$, and $R_S + R_{C1}$. This method, with the same V_{ch} restrictions as those indicated for the TPCM, can be used to find R_S from the following expression [4]:

$$R_S = \frac{T_{R_S+Rc1} - T_{Rc1}}{T_{Rc2+Rc1} - T_{Rc1}} R_{C2} \quad (4)$$

This expression is easier to evaluate than Equation (4), but the method has more inaccuracies in determining R_S [13].

A second variant of the TPCM, Figure 1c, uses an additional calibration resistor, R_{C3} , whenever low R_S measurements are needed. This means the circuit requires an additional charge and discharge process, but it allows R_S to be determined with 10 times greater precision if its value is around 10Ω [15].

Another resistive DIC, with a different arrangement of resistors, is shown in Figure 1d [16]. In this case, three charge and discharge cycles are also carried out. However, two pins detect changes from 0 to 1 during discharge through R_S , namely Ps and Pc1. Since Pc1 will always detect the change before Ps, there is an option to continue discharge from this moment of detection, either through R_S or $R_{C1} + R_{C2}$. This method reduces uncertainty due to quantization in T_{R_S} when the measurement value is low, which occurs if R_S is also low, thus achieving an improvement in accuracy by determining R_S for these resistance values. However, it comes at the expense of increased complexity of the equations that determine the value of R_S and the need to save two time measurements during the discharge of R_S .

Resistor R_p was introduced in these resistive DICs to reduce noise in the capacitor charge, thanks to the low-pass filter formed by R_p and C . However, as mentioned above, this solution has the disadvantage of increasing the time needed to charge C and, therefore, the total estimation time, $T_E(R_S)$. As indicated above, long charge times are needed since the maximum voltage the capacitor is charged at (V_{ch}) must be equal in all charge cycles and independent of the initial voltage each charge begins at ($V_C(0)$), meaning, for example, Equations (3) and (4) remain valid (the same is true for the circuits in Figure 1c,d). This can be seen in the charge equation of a capacitor through the Pp pin:

$$V_C(t) = V_{DD} + (V_C(0) - V_{DD})e^{\frac{-t}{(R_p+R_o)C}} \quad (5)$$

In this equation, the influence of $V_C(0)$ on the final voltage stored on the capacitor, V_{ch} , is only negligible if t is large.

However, the initial voltages may be different at the start of each charge process, since a series of PDD clock cycles may elapse between the moment transition $1 \rightarrow 0$ is detected during discharge and the moment discharge ends (normally the same number of cycles, n , for all discharges). In the case of readings in sensor arrays (where measurements are taken in parallel), this problem is further exacerbated since it is necessary to wait until all the sensors have been read if the charge process is synchronous. Figure 2 shows the effect that this additional time has on the final discharge voltage through two different resistors (the instants for the start of discharge of the two resistors have been superimposed in this figure for clarification). Since these final discharge voltages are the initial ones in the following charge processes, the latter initially show the same difference. The only condition necessary for this difference to appear is that the resistors used for discharge differ from each other. However, this is precisely what happens in all the above calibration methods, since, firstly, $R_{C1} \neq R_{C2}$ must always be met, and, secondly, R_S is usually different from the calibration resistors.

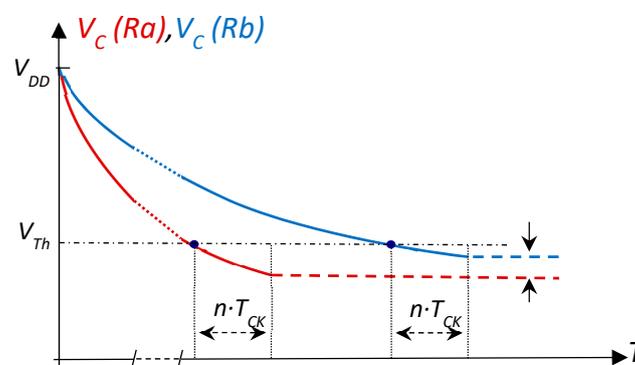


Figure 2. The C discharge process through two different resistors, R_a and R_b (curves $V_C(R_a)$ and $V_C(R_b)$) ends in different voltages due to the prolongation of the discharge for a certain number of clock cycles, $n \cdot T_{CK}$.

The following section presents a new resistive DIC that can reduce errors in estimating R_S , although the voltages the capacitor is charged at in each cycle differ from each other. This also allows shorter charge times, which in turn decreases $T_E(R_S)$.

3. Calibration Method for Reducing Error Due to Different Voltages Stored on the Capacitor of a Resistive DIC

To achieve that the initial values of the voltage on the capacitor do not affect the discharge process, we propose a new DIC that is shown in Figure 3. Three calibration resistors are used, R_{C11} , R_{C12} , and R_{C2} apart from the resistor that models the sensor, R_S , and the capacitor, C . The sum of the first two resistors will be called R_{C1} . This sum plays a role equivalent to the first calibration resistor in the TPCM. Moreover, resistor R_p , as used in the DICs of the previous section, is eliminated. The proposed DIC also requires three charge and discharge cycles (three measurement cycles) to estimate R_S . The charge cycles are performed by placing a logic 1 in all the PDD outputs in order to decrease the capacitor charge time, although this will be very similar to that needed if charging through P_p only. All discharges consist of two parts. In the first one, a partial discharge occurs through P_{c1} (i.e., through $R_{C1} = R_{C11} + R_{C12}$) for a preset time T_A . All other pins will be in the HZ state (inputs) during this time. T_A must meet the following relationship

$$T_X < T_A < T_{RC1} \quad (6)$$

where T_X is the time elapsed from the start of discharge through P_{c1} until voltage V_{Th} is reached in V_X . Since the voltage on the capacitor, at instant T_X , is

$$V_C(T_X) = \left(1 + \frac{R_{C11}}{R_{C12}}\right)V_{Th} \quad (7)$$

and, therefore, higher than V_{Th} ; discharge continues through P_{c1} up to T_A , without a logic 0 being detected in the P_p pin. The second part of the discharge begins as of T_A , continuing with R_S , R_{C2} , or R_{C1} itself, depending on the measurement cycle.

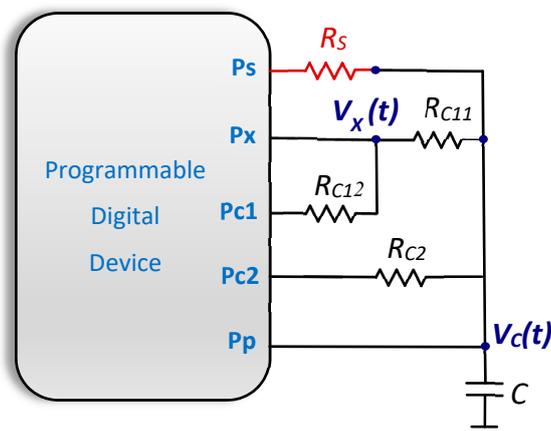


Figure 3. New resistive DIC proposed for error reduction due to different initial voltages stored on the capacitor (resistor/sensor to be estimated shown in red).

Bearing in mind that the initial discharge voltage may differ in each measurement cycle, it is necessary to distinguish between $V_{ch}(R_S)$, $V_{ch}(R_{C1})$, and $V_{ch}(R_{C2})$, and between $T_X(R_S)$, $T_X(R_{C1})$, and $T_X(R_{C2})$, where the resistor that the discharge finishes through in a specific measurement cycle is shown in brackets. Moreover, T_{R_S} , $T_{R_{C1}}$, and $T_{R_{C2}}$ maintain their meaning as the total discharge time up to $V_C = V_{Th}$ in each measurement cycle. However, T_{R_S} is now the sum of the time taken in the first part of the discharge through R_{C1} , T_A , plus the time taken in the second part of the discharge through R_S . Similarly, $T_{R_{C2}}$ is the sum of T_A and discharge time through R_{C2} . Moreover, $T_{R_{C1}}$ is the discharge

time through R_{C1} only, since both the first and second parts of the discharge take place through this resistor. The following variables will be used to set the equation for the new calibration method more straightforwardly: $T_{R_S}^*$, $T_{R_{C1}}^*$, and $T_{R_{C2}}^*$. These variables measure the time it would take for the resistor that appears in the sub-index of these variables to discharge C from T_X to $V_C = V_{Th}$ in the Pp pin (although these times are not measured in this calibration method). The times defined above, for the case of the R_S measurement cycle, are represented in Figure 4 (a similar figure would be achieved for the R_{C2} measurement cycle by changing R_S for R_{C2}).

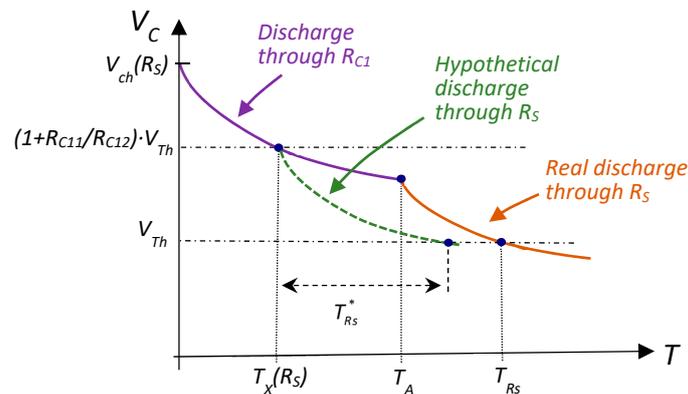


Figure 4. Times taken to estimate R_S in its measurement cycle. Actual discharge through R_S is shown in orange; in green is the length of a hypothetical discharge through R_S if started after a discharge through R_{C1} up to $T_X(R_S)$, $T_{R_S}^*$.

Only $T_{R_{C1}}^*$ can be found directly, since

$$T_{R_{C1}}^* = T_{R_{C1}} - T_X(R_{C1}) \quad (8)$$

However, T_R^* and $T_{R_{C2}}^*$ can only be found using the equation that describes the *Modified Discharge Process*, as introduced in [13]. This process is similar to the one described above, i.e., a capacitor is discharged through two resistors, R_i and R_j (first through R_i for time t_i , with discharging then ending through R_j for time t_j). Carrying out another capacitor discharge (from the same initial voltage to the same final voltage) through R_j only with discharge time T_j would allow us to know the time R_i would take to carry out the whole discharge, T_i , (without the need to carry out the discharge) by means of the equation (see Appendix A).

$$T_i = \frac{T_j \cdot t_i}{T_j - t_j} \quad (9)$$

The equivalent equation to this, considering the discharge shown in Figure 4 from instant $T_X(R_S)$, is given by

$$T_{R_{C1}}^* = \frac{T_{R_S}^*(T_A - T_X(R_S))}{T_{R_S}^* - (T_{R_S} - T_A)} \quad (10)$$

Thus:

$$T_{R_S}^* = \frac{T_{R_{C1}}^*(T_{R_S} - T_A)}{T_{R_{C1}}^* - T_A + T_X(R_S)} \quad (11)$$

Using this procedure when discharge ends through R_{C2} finds

$$T_{R_{C2}}^* = \frac{T_{R_{C1}}^*(T_{R_{C2}} - T_A)}{T_{R_{C1}}^* - T_A + T_X(R_{C2})} \quad (12)$$

Moreover, times $T_{R_S}^*$, $T_{R_{C1}}^*$, and $T_{R_{C2}}^*$ can be used to write a modified version of Equation (3) for three discharge cycles that start with the same capacitor voltage as shown in Equation (7), ending in V_{Th} .

$$R_S = \frac{T_{R_S}^* - T_{R_{C1}}^*}{T_{R_{C2}}^* - T_{R_{C1}}^*} (R_{C2} - R_{C1}) + R_{C1} \quad (13)$$

If the results of Equations (8), (11), and (12) are substituted in this expression, R_S can be estimated by the equation

$$R_S = \frac{\frac{T_{R_S} - T_A}{T_{R_{C1}} - T_A + T_X(R_S) - T_X(R_{C1})} - 1}{\frac{T_{R_{C2}} - T_A}{T_{R_{C1}} - T_A + T_X(R_{C2}) - T_X(R_{C1})} - 1} (R_{C2} - R_{C1}) + R_{C1} \quad (14)$$

All times are known in this equation, either because they have been measured, T_{R_S} , $T_{R_{C1}}$, $T_{R_{C2}}$, $T_X(R_S)$, $T_X(R_{C1})$, and $T_X(R_{C2})$, or because it has been established by the designer, T_A . The set formed by the new DIC proposed in Figure 3 and the new equation for calculating R_S (14) will be called the Short-Time Charging Calibration Method, SCCM.

The basic idea in this new calibration method is to convert a series of initial discharge voltages that can vary between measurement cycles, namely $V_{ch}(R_S)$, $V_{ch}(R_{C1})$, and $V_{ch}(R_{C2})$, into one indicated by Equation (7) that is constant and independent of the measurement cycle. Equation (14) needs more arithmetic operations and measurements than Equation (3), meaning it therefore has more sources of uncertainty. However, if the variation in the charge voltages of the three measurement cycles is large enough (which is indeed the case when shortening charge times to reduce $T_E(R_S)$), the new calibration method may provide better results than TPCM.

4. Experimental Results and Discussion

In order to study the proposed DIC and subsequently compare its results with those based on a classic calibration method such as TPCM, both circuits were implemented using a Xilinx FPGA, specifically the Spartan 6 XC6SLX25-3FTG256 model. The working voltage of the I/O blocks of this FPGA, and therefore, the maximum voltage on the capacitor for the discharges, V_{ch} , was 3.3 V. Output buffers were configured to drive up to 24 mA each. Time-to-digital conversion was performed by a 14-bit counter with a 20 ns time base, which allowed discharge times of up to 327.68 μ s. To achieve low measurement uncertainties, we have used the smart capture modules proposed in [28]. FPGA device utilization for the acquisition module was 2% of the Slice LUTs (329), 326 used as logic, and 3 used as route-thrus, and 1% of the Slice Registers (231), 223 used as Flip-Flops, and 8 used as latches. The choice of this device has been mainly due to the versatility of FPGAs. However, it is important to highlight that any PDD is a good candidate for the implementation of the method presented in this article, since no special characteristics of these circuits are required to work with these resistive DICs.

The tests were performed on a set of resistors in the range 270 to 7500 Ω , although the new SCCM allowed values of 10 k Ω to be reached in some of the experiments. As for the calibration resistors, the values chosen for SCCM were $R_{C11} = 557.46 \Omega$, $R_{C12} = 559.04 \Omega$, and $R_{C2} = 6165.9 \Omega$, while for TPCM, they were $R_{C1} = 1116.5 \Omega$ and $R_{C2} = 6165.9 \Omega$. Note that R_{C1} for TPCM is the sum of $R_{C11} + R_{C12} = 1116.5 \Omega$ used in SCCM. A 47 nF capacitor was chosen for C. The design rules for this type of DIC are fulfilled with these values, for both the calibration resistors and the capacitor used, as stated in the literature [23,29] (the value of R_{C1} is around 15% of the range of resistances to be measured and R_{C2} is around 85%). All the resistors were measured using an Agilent 34401A digital multimeter. In the case of the SCCM method, $T_A = 9.68 \mu$ s was established for partial discharge time through Pc1, thus complying with the restriction expressed in Equation (6).

In order to compare the results provided for the estimation of R_S using TPCM, as shown in Equation (3), and SCCM, as shown in Equation (14), several tests were carried out for both methods, with varying capacitor charge times. For the comparison, the TPCM has been slightly modified to ensure the capacitor charges as quickly as possible. Therefore, in TPCM, it was decided to charge

through all the available pins, as in SCCM. Furthermore, as resistor R_p in Figure 1a slows down the charge process, it was decided to replace it with a short circuit.

A 12-bit counter was implemented in the FPGA, $b_{11}b_{10}...b_1b_0$, to control the charge time in both methods. These bits will determine charge time. In order to simplify the hardware design in the FPGA, bearing in mind that a range of charge times must be implemented, the most significant output bit of this counter, b_{11} , was used to control maximum charge time, as indicated below. When the charge process starts, the counter resets, and the count starts. Charging continues as the counter advances, as long as b_{11} remains 0. The charge process (and the counter advance) ends at the moment b_{11} becomes 1, with the discharge process then starting. Therefore, the maximum charge time is $2^{11} \cdot T_{CK}$, where $T_{CK} = 20$ ns is the period of the clock signal used in the counter. In our case, this maximum charge time is therefore 40.96 μ s. Other counter output bits were used to find shorter charge times. For example, b_{10} was used as the control bit to find a charge time of 20.48 μ s. Bit pairs were used to make this control more precise when charge times were shorter. Therefore, the charge time was 1.92 μ s if the charge stops the first time bits b_6 and b_5 are simultaneously 1. The charge times used for the comparison between the two calibration methods were 1.92 μ s, 2.56 μ s, 3.84 μ s, 5.12 μ s, 10.24 μ s, 20.48 μ s, and 40.96 μ s. The figure of merit to be used for the comparison will be the maximum relative error found for the set of 500 estimations made for each resistor with each charge time.

The maximum relative errors found in the estimation of R_S with the charge times indicated above are shown in Figure 5 for both calibration methods. The results for the shortest charge time are shown in Figure 5a, with charge time increasing in the different figures up to Figure 5g, which shows the results for the longest charge time. Figure 5 shows two main features. Firstly, the maximum relative error with SCCM hardly varies between the different charge times. Indeed, for most resistors, this error varies between 0.5% and 0.3% and, only for very low resistance values, this error is higher with small charge times. This increase in the error for small resistances is caused by the quantization errors, since, in the case of SCCM, these errors are more severe because the time measurements of $T_X(R_S)$, $T_X(R_{C1})$, and $T_X(R_{C2})$ are smaller than T_{R_S} , $T_{R_{C1}}$, or $T_{R_{C2}}$. Obviously, this can be compensated by an increase in the clock frequency and/or the capacitance, C . However, these changes must be carefully evaluated considering the drawbacks that they entail (higher power consumption, increasing noise, and $T_E(R_S)$). Another more interesting way that could be used to achieve the reduction of quantization errors would be to use the method proposed in [16] together with the SCCM. However, this is beyond the objectives of this article.

Secondly, as expected, the maximum relative error in TPCM is large for small charge times, with a maximum of 12.4% for a charge time of 1.92 μ s and a resistance value of 7464 Ω . As the charge time increases, this error decreases for all resistance values in the range, until values slightly below 0.1% are reached for high resistances with a maximum charge time of 40.96 μ s. SCCM almost always outperforms TPCM in accuracy for short charge times up to 3.84 μ s. The exceptions to this are resistances of less than 600 Ω with a charge time of exactly 3.84 μ s. Relative errors in both methods are very similar for a charge time of 5.12 μ s. For higher charge times, TPCM slightly outperforms SCCM. However, even in these cases, the difference in the maximum relative errors is only 0.2% for almost the entire resistance range. Therefore, SCCM makes it possible to reduce the charge time more than 20-fold with a very moderate increase in error. Secondly, it is observed that SCCM allows higher resistance values to be estimated than in the case of TPCM. This is because part of the discharge through R_S is via R_{C1} , meaning that the total discharge time for $R_S > R_{C1}$ is shortened and discharges for higher resistance values can be measured with the designed counter.

The reason why error with high charge times is greater in SCCM than in TPCM is related to uncertainty in the measurement of T_X , $u(T_X)$, (independent of the measurement cycle, because to find T_X , the discharges are always through R_{C1}). Indeed [30] shows that uncertainty in measuring discharge time through any R , $u(T_R)$, depends proportionally on the circuit's electrical noise in the measurement node (in this case, the capacitor node), ϵ_C , and inversely on the absolute value of the derivative of the discharge curve (1) with respect to time at the measured instant.

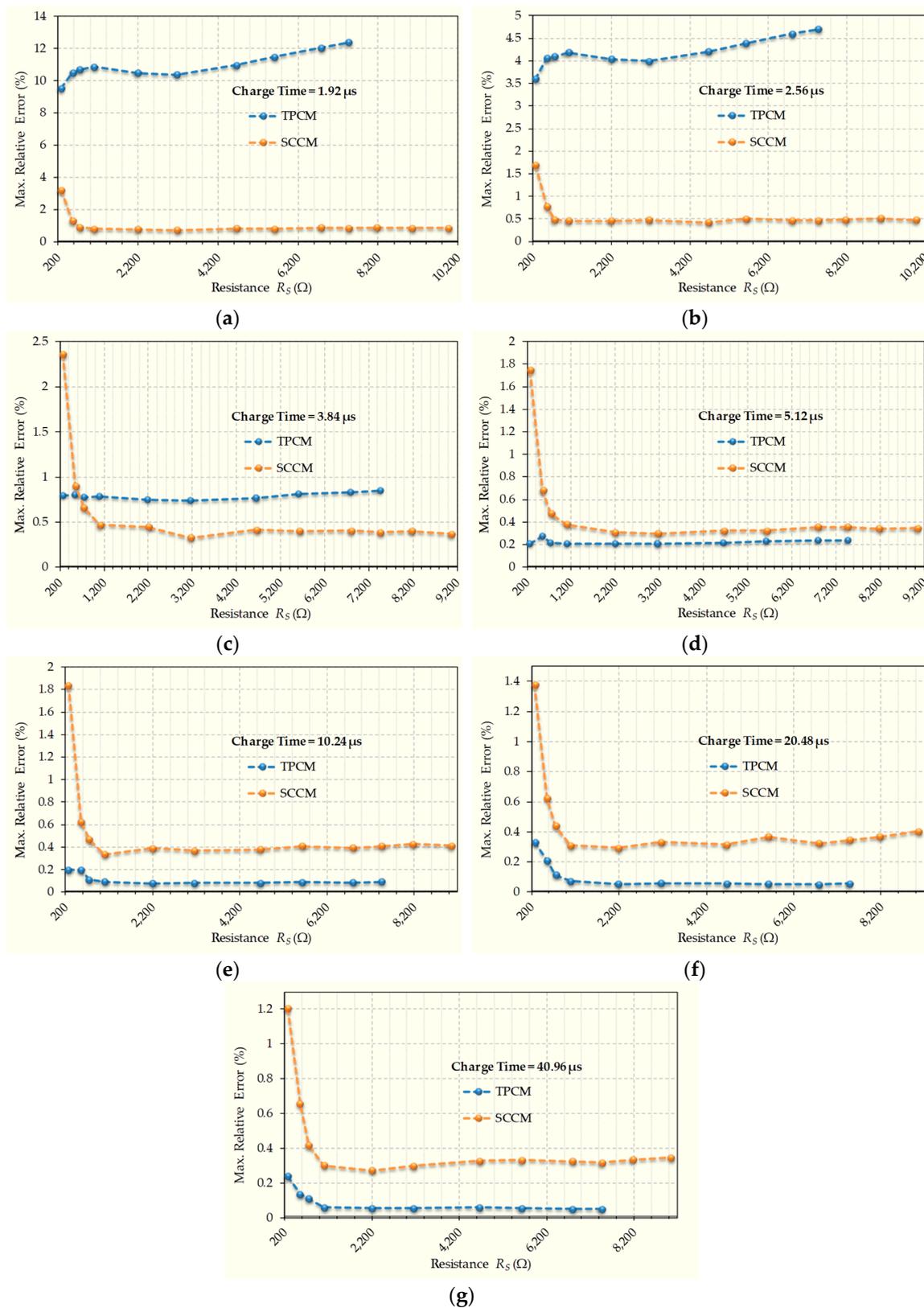


Figure 5. Comparison of maximum relative errors in estimating R_S when using the Short-Time Charging Calibration Method (SCCM) or TPCM. Each graph represents a different capacitor charge time. (a) charge time of 1.92 μs , (b) charge time of 2.56 μs , (c) charge time of 3.84 μs , (d) charge time of 5.12 μs , (e) charge time of 10.24 μs , (f) charge time of 20.48 μs , (g) charge time of 40.96 μs .

$$u(T_R) \propto \varepsilon_C \cdot (R + R_o) \cdot C \approx \varepsilon_C \cdot R \cdot C \quad (15)$$

Finally, as the $V_X(t)$ discharge curve in Figure 3 is given by

$$V_X(t) = \frac{R_{C12}}{R_{C1}} V_{ch} \cdot e^{\frac{-t}{(R_{C1} + R_o)C}} \quad (16)$$

it is easy to find that

$$u(T_X) \propto \varepsilon_X \cdot (R_{C1} + R_o) \cdot C \approx \varepsilon_X \cdot R_{C1} \cdot C \quad (17)$$

where ε_X is the electronic noise of node X in Figure 3. The relationship between $u(T_{Rc1})$ and $u(T_X)$ is therefore found by adapting Equation (15) and using Equation (17).

$$\frac{u(T_X)}{u(T_{Rc1})} \propto \frac{\varepsilon_X}{\varepsilon_C} \quad (18)$$

However, the electronic noise in node X is higher than that in the capacitor node, which is mainly due to the fact that the capacitor itself filters this noise. Therefore, the ratio in Equation (18) should be greater than one and approximately constant. Furthermore, the relationship between uncertainties will vary for each implementation of a single DIC. Figure 6 shows the results for $u(T_{Rc1})$ and $u(T_X)$ in our implementation of the circuit for the different charge times. Except for a small increase in $u(T_X)$ when the charge time is 1.92 μs , the uncertainties are approximately constant, since the resistance carrying out the capacitor discharge is the same in all cases, R_{C1} , and the relationship between these uncertainties is $u(T_X) \approx 4 \cdot u(T_{Rc1})$. The observed growth in uncertainty for a charge time of 1.92 μs is due to the final charging voltage already being much less than V_{DD} , and therefore T_X is a smaller value that is more affected by quantization errors. This high value of $u(T_X)$ compared to $u(T_{Rc1})$ is responsible for the maximum relative error of SCCM being higher than that of TPCM for longer charge times, especially considering that there are three times to be measured in node X, each with their corresponding uncertainties, as shown in Equation (14).

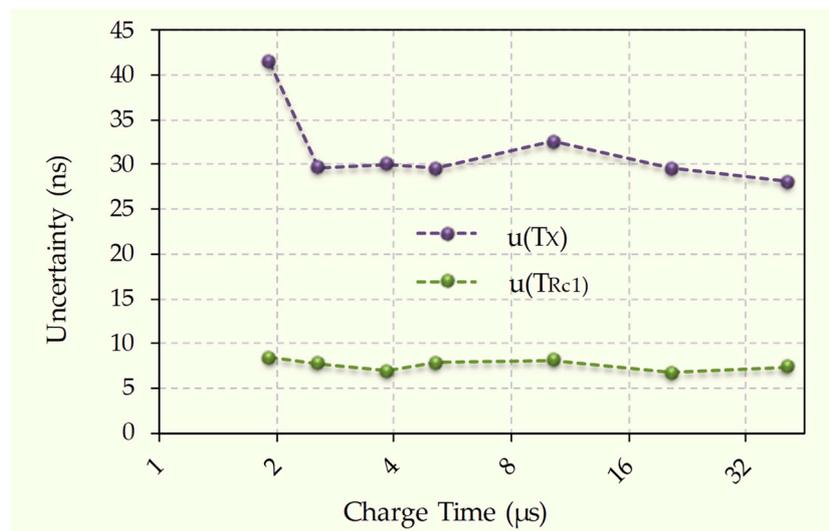


Figure 6. Comparison of uncertainties in discharge times measured in the capacitor node and in node X when discharge occurs through R_{C1} . Uncertainty in the capacitor node in Figure 3, $u(T_{Rc1})$, is shown in green, while uncertainty in the X node, $u(T_X)$, is shown in purple, both for different charge times (in log2 scale).

In order to compare the results for SCCM with those for TPCM, minimizing the influence of any uncertainty in the estimation of R_S , the average of the 500 estimations of R_S for each charge time has

been calculated, and this value has been taken as the systematic estimation of each method. We call the absolute difference between the real value of R_S and this systematic estimation systematic error. Figure 7 shows the difference between these systematic errors for both methods in the case of a charge time close to the minimum, $5.12 \mu\text{s}$, as shown in Figure 7a, and, for the maximum charge time, $40.96 \mu\text{s}$, as shown in Figure 7b. In Figure 7b, the systematic error is lower in SCCM (except for resistance value 556.4Ω), unlike the relative errors shown in Figure 5g. This shows that the main cause of errors in SCCM is the higher uncertainty of the different T_X measurements. The form of systematic errors in TPCM is typical, increasing with resistance value [30]. However, systematic errors increase more slowly in SCCM, meaning that the advantage for SCCM increases as the resistance value increases.

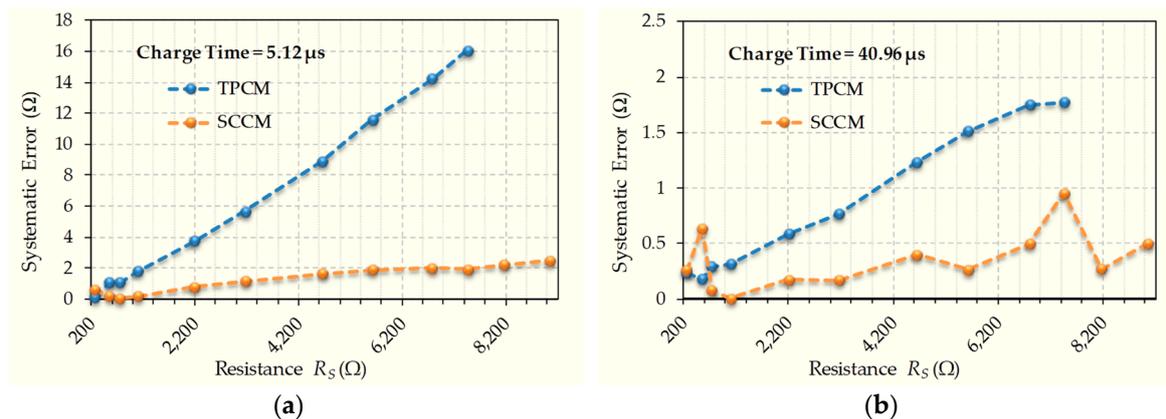


Figure 7. Systematic error for TPCM and SCCM for various charge times. (a) Charge Time of $5.12 \mu\text{s}$. (b) Charge Time of $40.96 \mu\text{s}$.

5. Conclusions

Direct Interface Circuits are a simple way to read a resistive sensor in digital form without the need for analog-to-digital converters. The simplest versions of these circuits need only a few passive elements (resistors and a capacitor) to provide this information, R_S . Even with these simple circuits, the accuracy achieved in measurement is quite high, with errors of just a few tenths of a percent. However, as in any circuit, they also have a series of limitations, most notably the time needed to carry out the estimation of R_S , $T_E(R_S)$. Since this time is the sum of various charge and discharge times, reducing each of them helps decrease $T_E(R_S)$.

Accuracy in the estimations when using a DIC is only possible if the final voltages stored on the capacitor are the same in the different charge cycles, which, since the initial voltages that charging starts from differ from each other, can only be achieved if capacitor charge times are long enough. This slows down the operation of the DIC, which can be a serious problem when multiple resistive sensors need to be read in a system.

This article presents a method to reduce charge times that consists of a new DIC architecture (in which only passive components are still used) together with a new calculation method for the estimation of R_S , which we call the Short-Time Charging Calibration Method, SCCM. The method is based on performing two measurements within a single discharge process, while a classic DIC only performs one. These new measurements only require an additional pin for the programmable digital device used in the DIC, and the information they provide means that the initial voltages in the discharge processes do not necessarily have to be the same in order to correctly estimate R_S . For charge times of $1.92 \mu\text{s}$, this method has achieved errors very similar to those in a classic DIC with charge times of $40.96 \mu\text{s}$, the difference being around 0.2%–0.3% for almost all resistance values in the tested range. Furthermore, SCCM can measure higher resistance values for the same maximum discharge time.

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Appendix A

If t_i , t_j , and T_j are the times defined in Section 3, then it is possible to find T_i using Equation (9). To demonstrate this, t_i , t_j , and T_j could be written as:

$$t_i = (R_i + R_o)C \ln\left(\frac{V_{ch}}{V_X}\right) \quad (A1)$$

$$t_j = (R_j + R_o)C \ln\left(\frac{V_X}{V_{Th}}\right) \quad (A2)$$

$$T_j = (R_j + R_o)C \ln\left(\frac{V_{ch}}{V_{Th}}\right) \quad (A3)$$

where V_X is the final voltage reached during the partial discharging through R_i . With these equations, we can write:

$$\begin{aligned} \frac{T_j \cdot t_i}{T_j - t_j} &= \frac{(R_j + R_o)C \ln\left(\frac{V_{ch}}{V_{Th}}\right) \cdot (R_i + R_o)C \ln\left(\frac{V_{ch}}{V_X}\right)}{(R_j + R_o)C \ln\left(\frac{V_{ch}}{V_{Th}}\right) - (R_j + R_o)C \ln\left(\frac{V_X}{V_{Th}}\right)} = \\ &= \frac{(R_i + R_o)C \ln\left(\frac{V_{ch}}{V_{Th}}\right) \ln\left(\frac{V_{ch}}{V_X}\right)}{\ln\left(\frac{V_{ch}}{V_{Th}}\right) - \ln\left(\frac{V_X}{V_{Th}}\right)} = (R_i + R_o)C \ln\left(\frac{V_{ch}}{V_{Th}}\right) = T_i \quad \square \end{aligned} \quad (A4)$$

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