

Article

Fully Integrated Light-Sensing Stimulator Design for Subretinal Implants

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Received: 20 November 2018; Accepted: 24 January 2019; Published: 28 January 2019



Abstract: This paper presents a fully integrated photodiode-based low-power and low-mismatch stimulator for a subretinal prosthesis. It is known that a subretinal prosthesis achieves 1600-pixel stimulators on a limited single-chip area that is implanted beneath the bipolar cell layer. However, the high-density pixels cause high power dissipation during stimulation and high fabrication costs because of special process technologies such as the complementary metal-oxide semiconductor CMOS image sensor process. In addition, the many residual charges arising from the high-density pixel stimulation have deleterious effects, such as tissue damage and electrode corrosion, on the retina tissue. In this work, we adopted a switched-capacitor current mirror technique for the single-pixel stimulator (SPStim) that enables low power consumption and low mismatch in the subretinal device. The customized P+/N-well photodiode used to sense the incident light in the SPStim also reduces the fabrication cost. The 64-pixel stimulators are fabricated in a standard 0.35- μm CMOS process along with a global digital controller, which occupies a chip area of $4.3 \times 3.2 \text{ mm}^2$ and are ex-vivo demonstrated using a dissected pig eyeball. According to measured results, the SPStim accomplishes a maximum biphasic pulse amplitude of 143 μA , which dissipates an average power of 167 μW in a stimulation period of 5 ms, and an average mismatch of 1.12 % between the cathodic and anodic pulses.

Keywords: subretinal prosthesis; photodiode; high-density pixels; ex-vivo demonstration; light sensor; digital controller; implantable device

1. Introduction

Retinal implants offer great promise for restoring vision to patients who suffer from retinal diseases such as retina pigmentosa and age-related macular degeneration. According to the anatomical position, retinal prostheses can be classified as epiretinal [1,2], subretinal [3–5], or suprachoroidal [6,7] devices. Among them, it has been reported that the subretinal implant can provide high pixel density of up to 1600 pixels [8], on a limited silicon chip area [9]; this is possible because the stimulator in the subretinal device does not need a high-resolution current-steering digital-to-analog converter (DAC) and its own local digital controller, which are employed to generate various biphasic current pulses for epiretinal and suprachoroidal prosthetics. The high-resolution DAC and the digital controller occupy a large area in a single-pixel stimulator (SPStim); the area becomes dominant with high-voltage CMOS (complementary metal-oxide semiconductor) process technology [2].

Figure 1a shows a subretinal prosthesis that is inserted into the subretinal space of the eye via ab-externo approach. The prosthetic chip and cable, which works to deliver a power and a command

data from an inductive coupling coil located in the retroauricular area, enters the subretinal space passing through the partial-thickness scleral flap. Then, the rest cable outside the eye is buried under the temporalis muscle. Figure 1b depicts the general architecture of a single-pixel stimulator (SPStim) for a subretinal implant, which is composed of a photosensor, a current amplifier, and a pulse shaper. A photodiode in the photosensor produces a dark current corresponding to the light intensity incoming onto the retina. The dark current is in the order of nano-amperes and has a monophasic shape. The current amplifier in Figure 1b works to amplify the dark current from tens to hundreds of microamperes. Finally, the pulse shaper reshapes the amplified monophasic signal to a biphasic current pulse, which consists of a rectangular cathodic and anodic pulse, and then delivers the biphasic signal into the bipolar cells interfaced with a microelectrode.

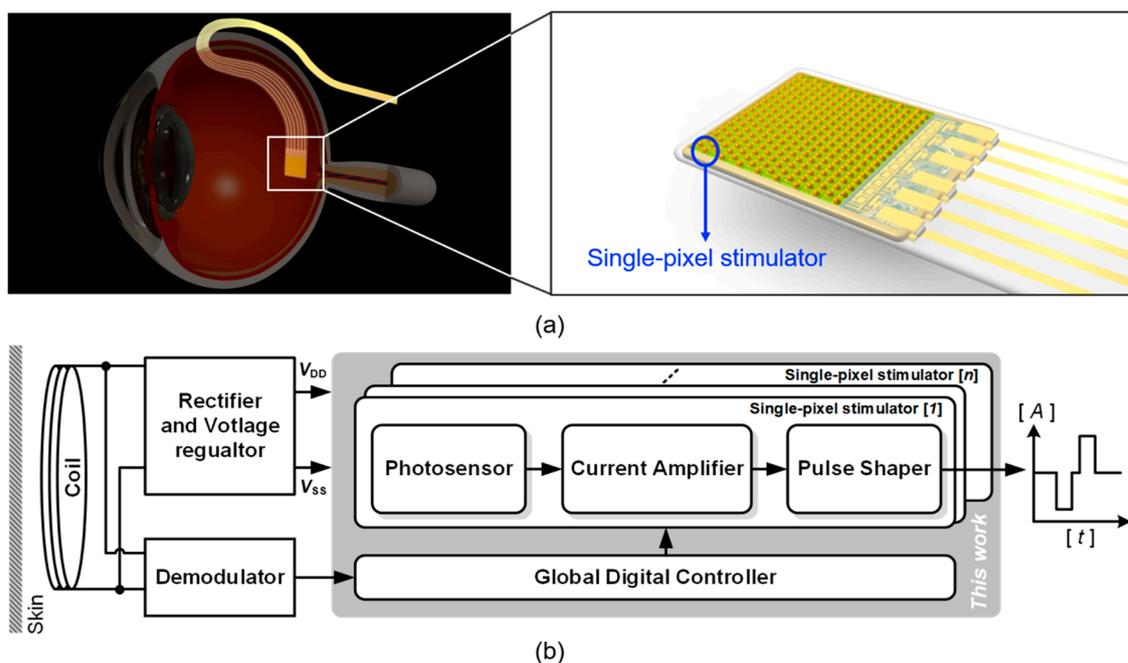


Figure 1. (a) System overview of a subretinal prosthesis that is implanted beneath the bipolar cell layer, (b) simplified architecture of the subretinal device including the single-pixel stimulator.

The single-pixel stimulator for the subretinal prosthesis should meet three design requirements as follows. First, the amplitude mismatch of the cathodic and anodic pulses should be as low as possible in order to reduce the residual charge on the retina tissue after stimulation. The residual charge sometimes induces unwanted spike excitation that results in tissue damage, as well as electrode corrosion that impedes the delivery of stimulation charge to the tissue from the stimulator output [10]. Thus, it is indispensable to minimize the amplitude mismatch of the biphasic stimulus current. Second, it must be fully controllable by digital logic embedded on the same chip in order to generate the diverse shapes of the biphasic stimulus current. Because visually impaired patients have individually different thresholds for exciting the nerves in the retina [11], after implantation, the stimulus current shapes must be adjusted, including the amplitude, width, period of the biphasic stimuli, and the interphase delay between the cathodic and anodic pulses. Finally, the stimulator necessitates a wide dynamic output range to produce various amplitudes of the biphasic current owing to the different thresholds of the patients to excite their retinal nerves. A simple way to widen the output dynamics is to raise the power supply rail. However, the high-voltage operation leads to high power consumption in the SPStim, which would become worse in a subretinal device with high-density pixels. We thus must devise a new SPStim architecture to accomplish the wide dynamic output range while maintaining low-voltage operation.

Over the last decade, a few single-pixel stimulators have been presented for subretinal implants to implement high-density stimulator arrays [3], low-voltage operation [12], and low mismatch [6,13]. To the authors’ best knowledge, however, any results that meet all of these design requirements have not yet been presented. Thus motivated, in this work we propose a SPStim design that adopts a switched-capacitor current mirror technique that achieves both low mismatch and wide dynamic output range in low-voltage operation. This stimulator circuit was fabricated in a standard 0.35- μm 4M2P CMOS process and ex-vivo demonstrated employing a dissected pig eyeball.

2. Methods

Figure 2 shows the circuit diagram of the proposed SPStim, which is composed of three stages: (1) a photosensor, (2) a current amplifier, and (3) a pulse shaper, as illustrated in Figure 1b. Also shown are simulated transient waveforms for the SPStim’s digital inputs and analog output. The photosensor stage is composed of a photodiode D_{PD} and a PMOS transistor M_1 , which works as a switch to reset D_{PD} . In this design, a customized photodiode that has the structure of a P+ and N-well as illustrated in Figure 2a has been employed because of its high sensitivity [14] and relatively low fabrication cost compared with the CMOS image sensor process that requires a deeper epitaxial layer, anti-reflective coating and optimization of passivation in order to minimize interference [15]. D_{PD} can be modeled as a dark current source I_{DARK} , which is proportional to the incident light intensity, and a parasitic capacitor C_{PD} , which arises from the junction area of the P+ and N-well in the diode, C_{gd1} , C_{gs3} , C_{gs2} , and C_{gs2} . Here, C_{gd} and C_{gs} denote a gate-drain and gate-source parasitic capacitance of the transistors. Although I_{DARK} and C_{PD} respectively vary with the light intensity and the dimension of D_{PD} and its adjacent transistors, we set I_{DARK} and C_{PD} to 8 nA and 6 pF for the simulation environment.

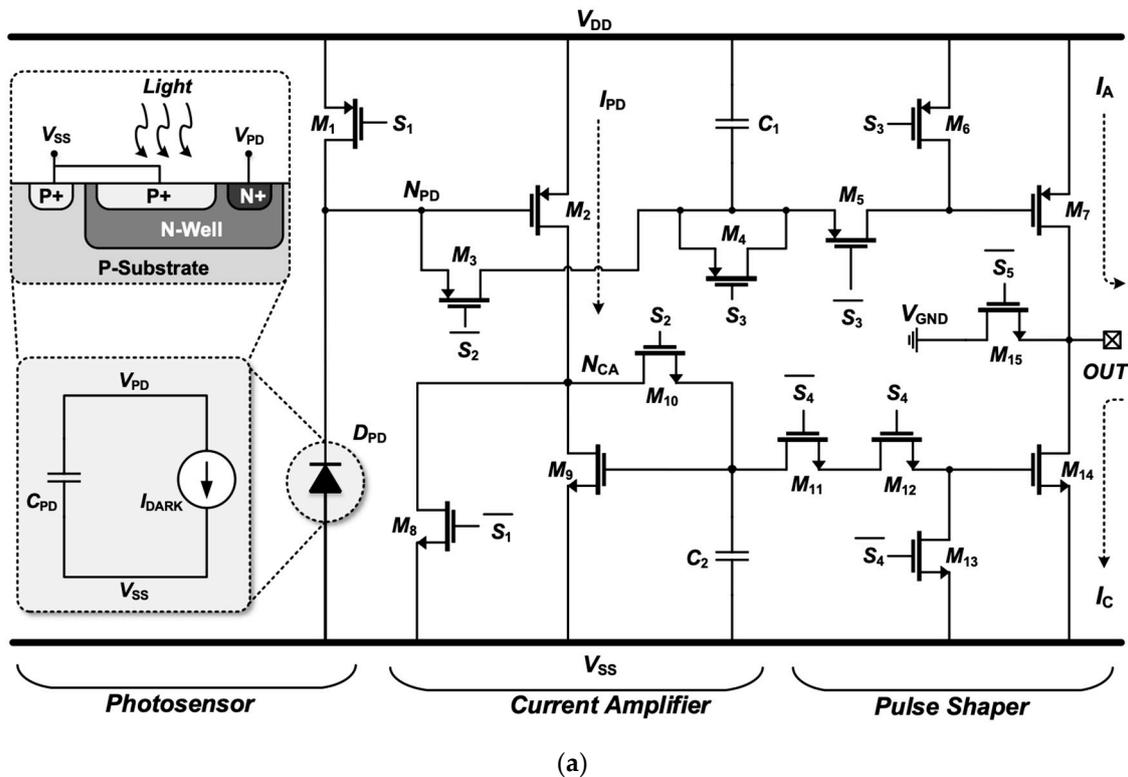


Figure 2. Cont.

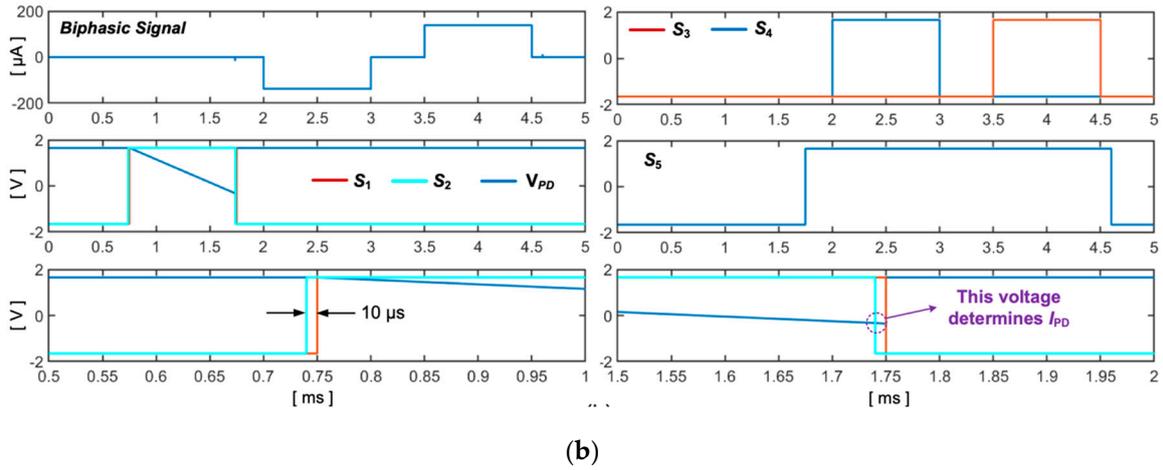


Figure 2. (a) Circuit diagram of the proposed single-pixel stimulator adopting a customized photodiode and a switched capacitor current mirror technique; (b) simulated transient waveform to show input and analog output.

The proposed SPStim operates in four different modes: the preset mode (0–0.74 ms in Figure 2b), reset mode (0.74–0.75 ms), charging mode (0.75–1.75 ms), and stimulation mode (0.175–4.6 ms), followed by the next preset mode (0.46–5 ms). During the preset mode, where all signals of the digital controller are set to logic 0, the PMOS transistor M_1 is fully turned on, and as a result, C_{PD} is charged up to V_{DD} . The stages other than the photodiode stage are deactivated in this mode to diminish unnecessary power dissipation. By applying a logic 1 to the S_2 on M_3 and M_{10} in the current amplifier stage, the reset mode begins, where the capacitors C_1 and C_2 are reset to V_{DD} through M_1 and M_3 , and to V_{SS} through M_8 and M_{10} , respectively. Thus, the previous stimulation memory recorded on C_1 and C_2 is erased so as to receive new stimulation information.

The charging mode starts when the S_1 on M_1 and M_8 becomes logic 1. The S_1 is synchronized with the S_2 , but its rising and falling edges lag those of the S_2 by 10 μs . We generate the S_1 from the S_2 using a simple delay chain as presented in [16]. As the S_1 turns high, the transistor M_1 is immediately disabled. Because of the I_{DARK} , the node voltage of N_{PD} , here called V_{PD} , begins to steadily drop from V_{DD} to $V_{DD} - I_{DARK} \times \Delta T / (C_1 + C_{PD})$, where ΔT indicates the duration of the charging mode (0.75–1.75 ms in this simulation). The drop in V_{PD} enables the PMOS transistor M_2 , thereby entering it to a saturation region. Accordingly, the current I_{PD} generated from M_2 can be defined as

$$I_{PD} = \frac{1}{2} \mu_P C_{OX} \left(\frac{W}{L} \right)_2 (V_{DD} - V_{PD} - |V_{TH,P}|)^2 = \frac{1}{2} \mu_P C_{OX} \left(\frac{W}{L} \right)_2 \left(\frac{I_{DARK} \times \Delta T}{C_1 + C_{PD}} - |V_{TH,P}| \right)^2 \quad (1)$$

Here, μ_P , C_{OX} , W/L , and $V_{TH,P}$ are the channel mobility, gate oxide capacitance per unit area, aspect ratio, and PMOS threshold voltage, respectively. This equation shows that the small current I_{DARK} in the nano-ampere range is amplified to a stimulus current in the tens to hundreds of micro-amperes by adjusting the charging duration ΔT . In this work, we aimed to generate a stimulation current of 150 μA at maximum. Because I_{PD} produced from M_2 flows out to V_{SS} only through M_9 , I_{PD} can be transformed to:

$$I_{PD} = \frac{1}{2} \mu_P C_{OX} \left(\frac{W}{L} \right)_2 (V_{DD} - V_{PD} - |V_{TH,P}|)^2 = \frac{1}{2} \mu_N C_{OX} \left(\frac{W}{L} \right)_9 (V_{CA} - V_{TH,N})^2 \quad (2)$$

Here, μ_N and V_{CA} denote the channel mobility of NMOS transistor and the node voltage of N_{CA} , respectively. V_{CA} can be rewritten as:

$$V_{CA} = \sqrt{\frac{2I_{PD}}{\mu_N C_{OX} \left(\frac{W}{L}\right)_9}} + V_{TH,N} \quad (3)$$

Including I_{PD} , V_{CA} changes with the incident light intensity and ΔT . Consequently, the voltages V_{PD} and V_{CA} are correlated with I_{PD} , which is used as the stimulus current, and are recorded on C_1 and C_2 at 1.74 ms in Figure 2b when the S_2 turns back to a logic 0. After 10 μ s, the S_1 turns off again. Here, the 10- μ s delay reduces the deleterious effect of charge injection that can lead to voltage fluctuations on C_1 and C_2 by the S_1 switching.

The stimulation mode starts when the S_5 signal turns to a logic 1 at 1.75 ms in Figure 2b. In other modes except for this stimulation one, the PMOS transistor M_{15} always stays “on” to prevent DC current from being leaked out to the retina tissue. By turning the S_4 to a logic 1, the V_{CA} stored on C_2 is applied to the gate of the NMOS transistor M_{14} , thereby generating a cathodic current I_C :

$$I_C = \frac{1}{2} \mu_N C_{OX} \left(\frac{W}{L}\right)_{14} (V_{CA} - V_{TH,N})^2 \text{ and thus } \frac{I_C}{I_{PD}} = \frac{\left(\frac{W}{L}\right)_{14}}{\left(\frac{W}{L}\right)_9} \quad (4)$$

Here, the channel-length modulation effect can be reduced by enlarging the length of M_{14} while still making the aspect ratio $(W/L)_{14}$ equal to $(W/L)_9$. In order to generate an anodic current pulse, the conventional designs exploit an additional current-mirror branch [4,6,12,13]. This results in unnecessary power consumption and a large mismatch between the cathodic and anodic currents.

Under the assumption that the additional current-mirror branch to copy I_{PD} for I_A exits in Figure 2a, the average power that the SPStim dissipates can be approximated to:

$$P_{av} \approx \underbrace{\frac{1}{T_S} \int_0^{T_S} I_{PD} \times (V_{DD} - V_{SS}) dt}_{\text{Current Amplifier}} + \underbrace{\frac{1}{T_S} \int_0^{T_S} [I_A \times V_{DD} - I_C \times V_{SS} + I_C \times (V_{DD} - V_{SS})] dt}_{\text{Pulse Shaper}} \quad (5)$$

Here, I_{DARK} is ignored because of $I_{PD} \gg I_{DARK}$ and T_S denotes the period of the biphasic waveform. In the second term of Equation (5), $I_C \times (V_{DD} - V_{SS})$ arises from the additional branch. Thus, the average power dissipated by all mirroring branches can be written as:

$$P_{tot,branch} \approx N \times \frac{1}{T_S} \int_0^{T_S} I_C \times (V_{DD} - V_{SS}) dt \quad (6)$$

where N means the number of pixels simultaneously stimulated. N also becomes higher in a subretinal device with high-density pixels.

By adopting the capacitor C_1 to directly record the value of V_{PD} , in this work, we remove the need for the additional branch, thus reducing both mismatch and power dissipation. As a result, the average power of the SPStim can be approximately expressed as:

$$P_{av} \approx \underbrace{\frac{1}{T_S} \int_0^{T_S} I_{PD} \times (V_{DD} - V_{SS}) dt}_{\text{Current Amplifier}} + \underbrace{\frac{1}{T_S} \int_0^{T_S} (I_A \times V_{DD} - I_C \times V_{SS}) dt}_{\text{Pulse shaper}} \quad (7)$$

This equation shows that the proposed SPStim consumes relatively less power compared to a stimulator using the addition current-mirror branch.

After the cathodic pulse, a logic 1 is applied to the PMOS transistor M_5 , and then the V_{PD} produces the anodic current I_A from M_7 . The dummy transistors M_4 and M_{11} are also harnessed to avoid charge injection caused by the M_5 and M_{12} switching. Consequently, the two switched-capacitor current mirrors adopted in the proposed SPStim make it possible to reduce power consumption in high-density pixel array; reduce the mismatch, which allows low residual charge on the tissue after stimulation; and widen the output dynamic range, which enables low-voltage operation.

3. Measurement

Figure 3 shows a micrograph of the 64-pixel stimulator array adopting the proposed architecture, and the global digital controller to produce digital signals for S_1, S_2, S_3, S_4 and S_5 in Figure 2a; both were fabricated in a single chip using a standard 0.35- μm 4M2P CMOS process. This full chip occupies an active area of $4.3 \times 3.2 \text{ mm}^2$. We first conducted a benchtop experiment to measure the transient biphasic current waveforms, which vary with the incident light intensity, using a light source (Model: Newport 66088-LED). Figure 4a illustrates the biphasic current waveform and its digital control signals observed with an oscilloscope (Model: Tektronix MSO4104). By changing the light intensity and supplying various digital pulses to the SPStim, we successfully generated diverse biphasic current shapes in amplitude, width, interphase and period. In this benchtop experiment, we used a 10-k Ω resistor to simply mimic the electrode resistance and set the time width for S_2 to 2 ms for fair comparison of the light-dependent biphasic current amplitudes.

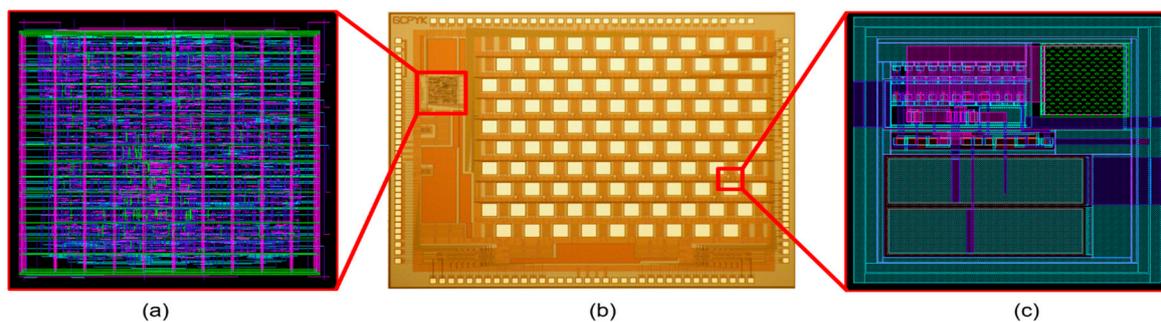


Figure 3. (a) Layout of the global digital controller embedded onto the signal chip with a 64-pixel stimulator array (its active area is gauged as $441.5 \times 425.5 \mu\text{m}^2$); (b) micrograph of the 64-pixel stimulator array; (c) layout of the proposed single-pixel stimulator, which occupies an active area of $114 \times 117 \mu\text{m}^2$.

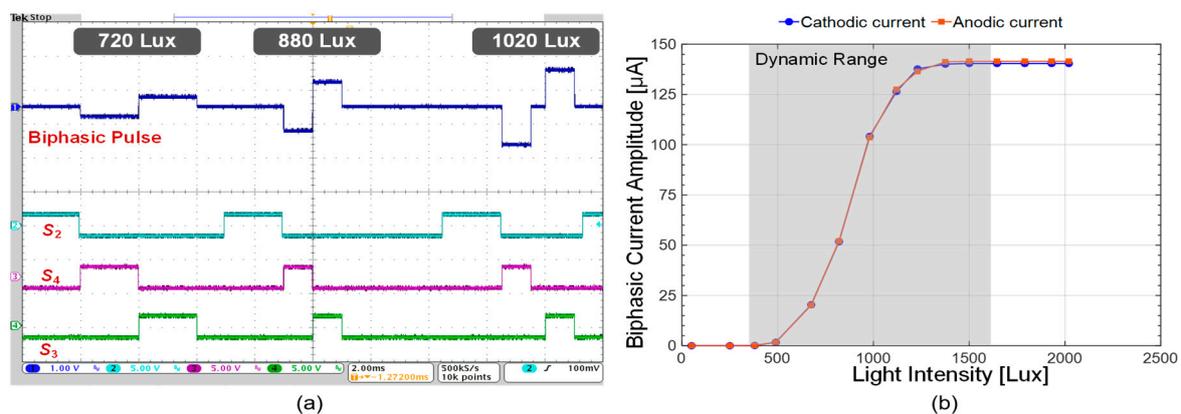


Figure 4. (a) Measured transient waveforms for the biphasic current and digital input pulses, where a 10-k Ω resistor was used to model the electrode resistance; (b) anodic and cathodic current amplitudes varying with incident light intensity.

Figure 4b shows the measured anodic (red line) and cathodic (blue line) amplitudes relying on the incident light intensity.

The observed results show that the biphasic stimulus current of the proposed SPStim varies from 0 to 143 μA in the dynamic range from 400 to 1600 lux, where an average mismatch of 1.12% was calculated using the following equation.

$$\text{Mismatch} = \frac{1}{N} \sum_{n=1}^N \frac{|A_{\text{anodic}}(n) - A_{\text{cathodic}}(n)|}{\max[A_{\text{anodic}}(n), A_{\text{cathodic}}(n)]} \quad (8)$$

Here, N , A_{anodic} and A_{cathodic} indicate the number of measured samples, the anodic and cathodic pulse amplitudes in the dynamic range. This low mismatch is due to the switched-capacitor current mirror technique described in Figure 2a. The charge remaining on the tissue after stimulation was completely removed by turning on the charge-balancing switch M_{15} .

Next, we ex-vivo demonstrated the proposed SPStim using a dissected pig eyeball as shown in Figure 5. Here, it is observed that the biphasic pulse amplitudes are reduced by approximately 29% compared to the waveforms measured in Figure 4a. This is because the incident light intensity is attenuated when passing through the pig eyeball lens [17]. In terms of Equation (1), the attenuated light reduces I_{DARK} in the photodiode, thereby reducing the stimulation current I_{PD} . To compensate for the reduced I_{PD} , we elongated the S_2 (ΔT in Equation (1)) from 2 ms (see Figure 4a) to 2.5 ms, and as a result, the SP-Stim could generate the same biphasic pulse amplitudes as observed in Figure 4b in the same dynamic range. This demonstration shows that the customized global digital controller is necessary to adjust biphasic stimulus pulses after implantation. Finally, the overall performance of the proposed SPStim is summarized in Table 1.

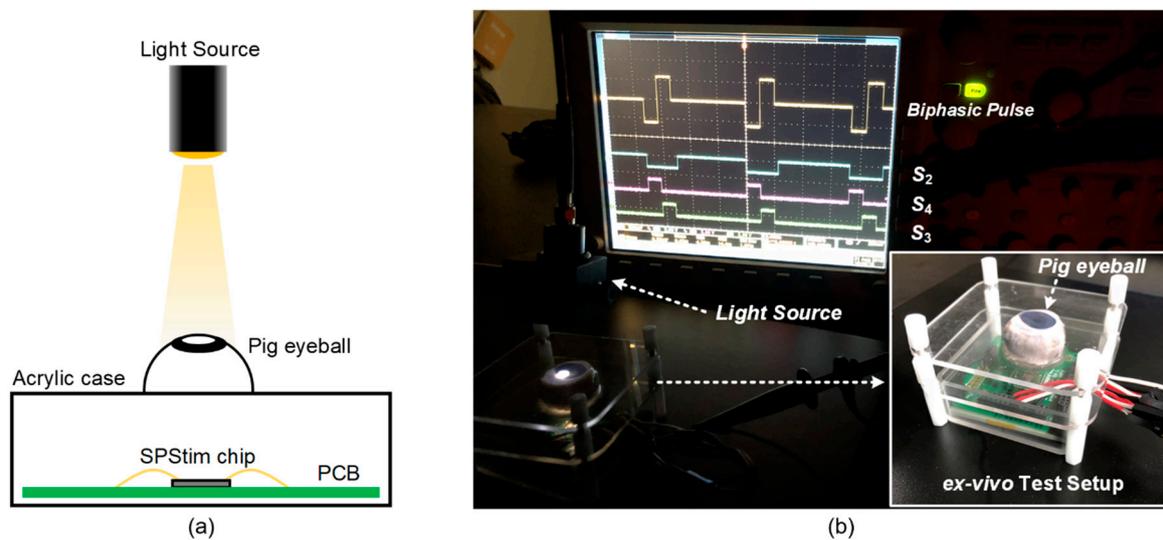


Figure 5. (a) Illustration of the ex-vivo demonstration setup; (b) ex-vivo experiment using a dissected pig eyeball.

Table 1. Electrical performance Summary and comparison of the proposed single-pixel stimulator (SPStim).

	[18]	[6]	[12]	[13]	[3,18–20]	This Work
CMOS Process	0.35- μm standard	0.18- μm CIS **	0.18- μm CIS **	0.35- μm BCD ***	0.35- μm CIS **	0.35- μm standard
Supply voltage [V]	5	± 1.65	0.5, 1.8	5, 12	± 2	± 1.65
Chip area [mm^2]	1.0×2.7	2.2×2.2	1.9×1.9	2.5×1.2	3×3.5	4.3×3.2
Single pixel area [μm^2]	200×200	127×167	30×30	55×50	30×30	114×117
Dynamic range [Lux]	-	400–1200	1–1000	100–250	0.1–10,000	400–1600
Pulse amplitude * [μA]	50–1050	0–343	0–50	0–300	0–100	0–143
On-chip digital controller	Yes	No	Yes	No	Yes	Yes
Pulse width * [ms]	-	-	-	-	4	0.5–5
Pulse period * [ms]	-	-	60	-	3–100	1–50
Interphase delay * [ms]	-	-	-	-	0 ms	0–2 ms
Mismatch [%]	-	4.85	-	-	-	1.12
Stimulation method	Charge-balanced biphasic current stimulation					

* Pulse: Biphasic Pulse, ** CIS: CMOS Image Sensor, *** BCD: Bipolar CMOS and Double diffused MOS(DMOS).

4. Conclusions

A fully integrated low-power and low-mismatch SPStim was designed for subretinal implants. By adopting two switched-capacitor current mirrors for anodic and cathodic pulse generation, in this work, we achieved relatively less power consumption, compared to a SPStim using the additional current-mirror branch to generate an anodic or a cathodic stimulation pulses, and low mismatch to decrease the residual charges that can have deleterious effects on the retina. Using the customized P+/N-well photodiode in a standard CMOS process also enabled relatively lower fabrication cost than a complex CMOS images sensor process. The 64-pixel stimulators employing the proposed architecture were fabricated in a standard 0.35- μm CMOS process and ex-vivo tested with a dissected pig eyeball. From the measured results, the device achieves a maximum biphasic pulse amplitude of 143 μA , an output dynamic range of 86.7%, and a mismatch of 1.12% on average between the anodic and cathodic pulses. The customized global digital controller, for producing diverse biphasic stimulus currents in amplitude, width, interphase delay, and period, was embedded on the same chip with the 64-pixel stimulators and used to compensate for the attenuated light intensity passing through the pig eyeball lens in ex-vivo experiments. In future work, a refined 64-pixel stimulator array will functionalize the wireless power and data telemetry that we are developing now.

Author Contributions: The individual contributions of authors are follows: H.K. designed the stimulator chip and wrote the manuscript. W.H.A. designed the on-chip digital controller and took part in the manuscript revision. S.-W.K. conducted the ex-vivo experiment using the dissected pig eyeball. J.K. managed the project.

Funding: This research was partially supported by the National Research Foundation of Korea (Grant No. NRF-2017M3A9E2056461) and the Gachon University Gil Medical Center (Grant No. 2016-16).

Acknowledgments: The authors are grateful to the IC Design Education Center (IDEC) for chip fabrication.

Conflicts of Interest: The authors declare no conflict of interest.

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